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VOICE OF THE ENGINEER

AUG 17

Issue 17/2006

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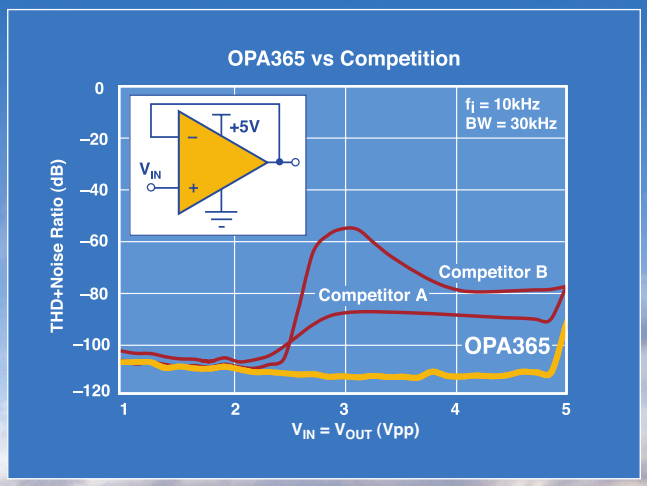
Low Noise Low Distortion

Zero-Crossover, 50MHz, Rail-to-Rail Amp

The OPA365 amplifier utilizes an innovative zero-crossover, single input stage architecture to deliver glitchless rail-to-rail performance with ultra-low distortion (0.0006% THD+N). Also featuring low noise (4.5nV$\sqrt{Hz}$) and high-speed operation (50MHz gain bandwidth), the device is ideal for a wide range of single-supply applications in portable instrumentation, data acquisition, audio, portable medical, test and measurement systems.



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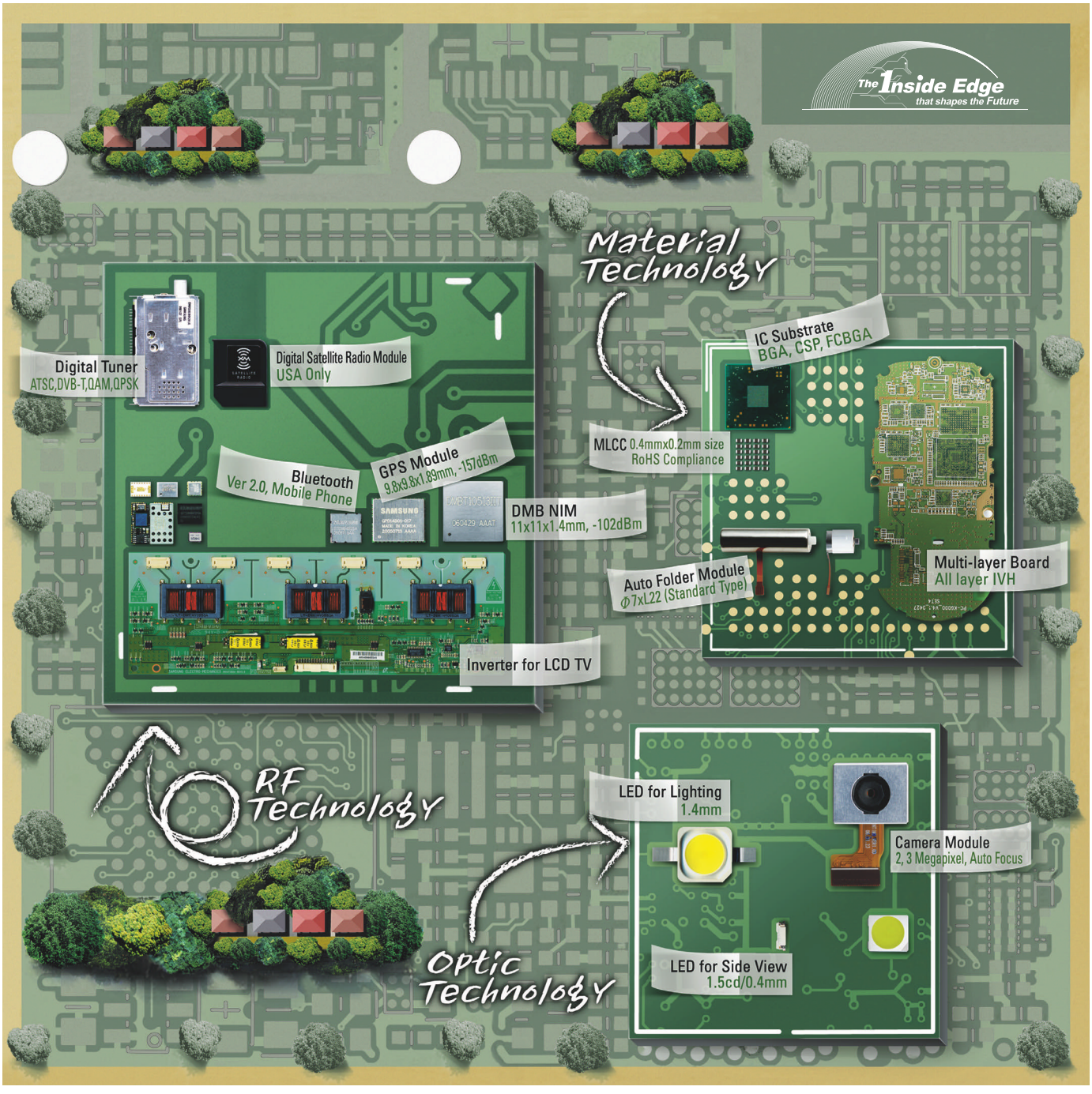


The 1nside Edge that shapes the Future

Samsung Electro-Mechanics (Samsung) has started up production of **LEDs** for lighting as well as mobile phones, car navigators, PMPs and Note PCs.

SB Byun (sbbyun@samsung.com, 949-797-8054)

Samsung has brought out 2, 3 Megapixel **camera module** with auto focus function.

JIM Park (jimpark@samsung.com, 847-549-9421)

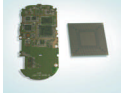
Samsung has produced digital tuners compatible with all broadcasting signals worldwide, for TV, Set-top boxes and mobile phones, as well as a variety of micro-sized RF components, **Bluetooth, wireless LAN, GPS Module, FEM,** etc., that support the portability of mobile devices.

JS Han (han.jungsuk@samsung.com, 201-229-6096)

Samsung has completed development of world's first 0402(0.4X0.2mm) **MLCC**, as thin a human hair, which uses copper nickel, palladium as

internal electrode material. Specifically, 0402 Cu MLCC has better high frequency performance than others.

Peter Kang (semksk@samsung.com, 949-797-8017)



Samsung has offered **multi-layer boards** named,'SAVIA™(Samsung Any Via)', which have all-layer IVH characteristics and **Flip Chip substrate.**

Wes Sohn (wansohn@samsung.com, 480-592-0180)

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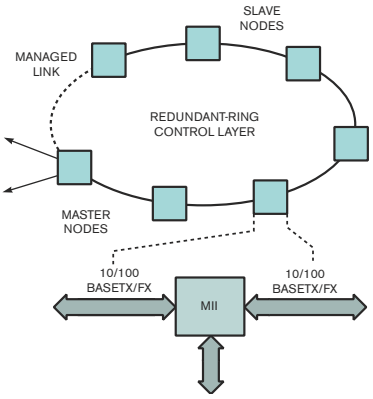
Sifting the DFM players

Smart-building systems converge



Designing Ethernet into industrial applications

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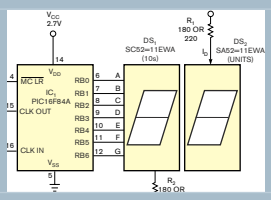

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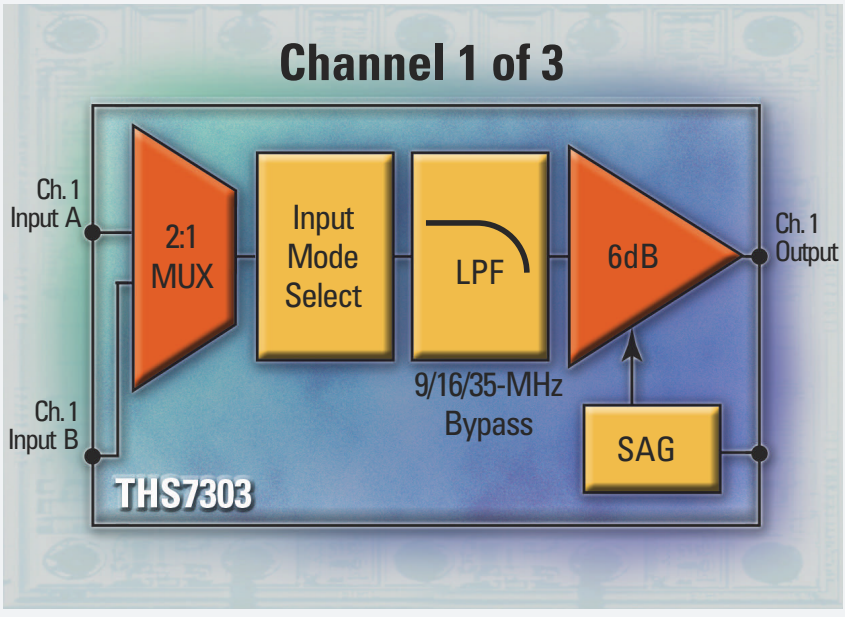
3-Ch. Low-Power Video Amp with I²C Control



▶ Applications

- Set-top boxes
- Digital televisions
- Personal video/DVD recorders
- Portable USB devices

▶ Features

- 2.7V to 5V single-supply operation
- Low power consumption: 55mW at 3.3V
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THS7353	3	9, 16, 35	5	150	0, Adjustable	AC-Bias, AC-STC, DC, DC+Shift	AC or DC	No	$1.65

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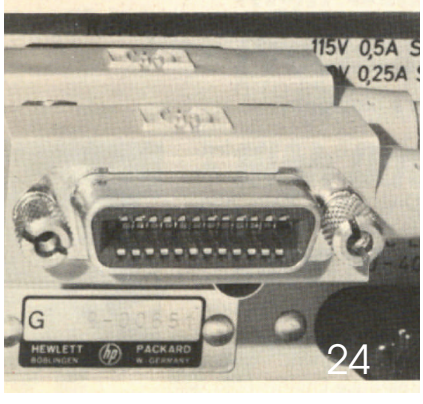

DEPARTMENTS & COLUMNS

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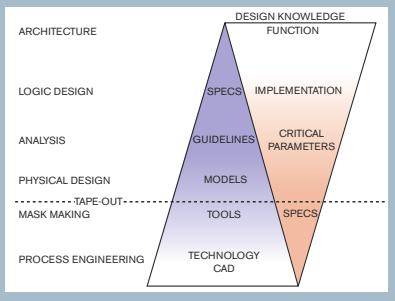

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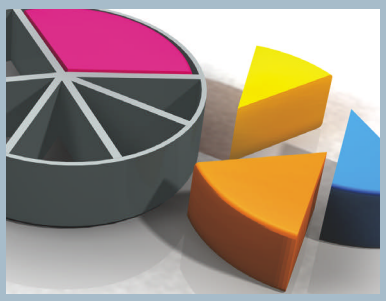

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BY MAURY WRIGHT, EDITOR IN CHIEF

Editorial ethics: meeting the ASBPE's transparency mandate

I just got back from a trip that included two days at the ASBPE (American Society of Business Publication Editors) National Editorial Conference, at which editorial-ethics issues were hot topics. At the conference, the ASBPE (www.asbpe.org) unveiled its *Guide to Preferred Editorial Practices*. A mandate for "ethics-guide transparency" appears on the first page of the guide, and speakers at the conference stressed this subject. The guide states, "ASBPE urges publishers and editors to make their ethical standards transparent both for its internal staff and externally for its readers, advertisers, and others in their markets." Although *EDN* operates with high regard for ethics, I'm not sure that we've ever explicitly defined our policies to you, the readers, so here goes.

A couple of years ago, our parent company, Reed Business, formally adopted the ASME (American Society of Magazine Editors) Guidelines (www.magazine.org/editorial/guidelines). Reed Business stipulates that all publications must abide by the ASME document. We also have an internal editorial board that both augments ASME and watches over the actions of our titles. *EDN* may also adopt or follow the ASBPE guide in areas that the ASME doesn't cover and vice versa.

I'd like to briefly highlight a few details that are important for *EDN* to earn your trust as a source of information. At the highest level, we simply never consider who advertises when we write features, columns, new products, or any other type of article. But we take additional steps to ensure that there is no illusion of collusion. For example, we never allow an advertiser to buy an ad opposite an editorial mention. A vendor might know that one of its engineers has a bylined article scheduled for an upcoming issue, but we don't allow that vendor to place an ad in the pages of that contributed article. The only reason that you might in some instances see an ad adjacent to an editorial mention would be that the vendor had previously contracted for the same "position" in each issue or every other issue. For example, an advertiser could buy a position in the Pulse section. On occasion, a Pulse article might mention that advertiser.

We also seriously consider the issues of our masthead and staff. Some publications list freelance or contract writers as if they were staff members. ASME mandates that we convey the titles only of full-time staff. We identify any contractors as "contributing editors." Some publications also use staff editors to write advertiser-sponsored content, such as supplements and advertorials; however, we don't allow our staff members to work on projects wherein an advertiser dictates the content.

We are also careful about accepting benefits, such as paid travel from vendors or trade associations. Vendors frequently offer to pay for airfare and hotel accommodations for an *EDN* editor's visit. We don't accept such offers when the vendor makes them only to *EDN*. We sometimes accept travel reimbursement when a company offers travel to *EDN* and broadly to all of our competitors. At the ASBPE conference, however, I learned that we should disclose the acceptance of reimbursement in any article that eventually evolves from such a trip.

The same rules that apply to our magazine apply to our Web site, e-mail newsletters, and any other media that we use. The online area is one in which some publishers are loosening their ethics policies. Please contact me if you ever think we've failed to live up to our ethics commitment. I want to know.

Also at the ASBPE conference, *EDN* picked up some ASBPE National Azbee awards for magazines with circulation of more than 80,000 readers (see **sidebar** "*EDN*'s Azbee wins").EDN

You can reach me at 1-858-748-6785 or mgwright@edn.com.

EDN's AZBEE WINS

- **Gold Award, Regular Department: "Prying Eyes," *EDN*, June 9, 2005 (www.edn.com/article/CA605509), July 7, 2005 (www.edn.com/article/CA621643), and Aug 4, 2005 (www.edn.com/article/CA629314).**
- **Bronze Award, Computer Generated Front Cover: "Who are you buying your EDA software from?" *EDN*, Aug 18, 2005 (www.edn.com/toc-archive/2005/20050818.html).**
- **Bronze Award, Publication Redesign: "Song Wars," *EDN*, June 9, 2005 (www.edn.com/toc-archive/2005/20050609.html.**

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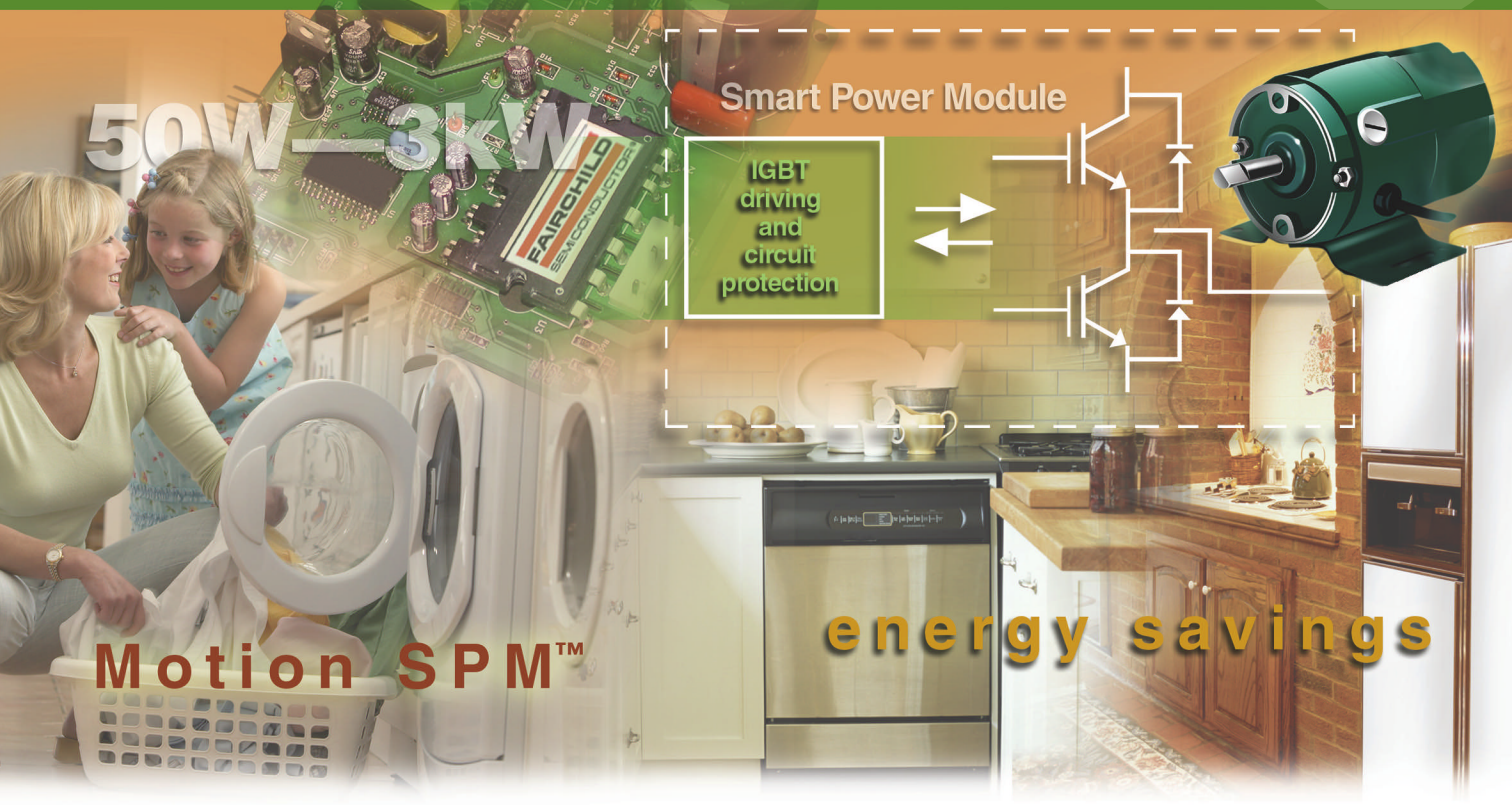

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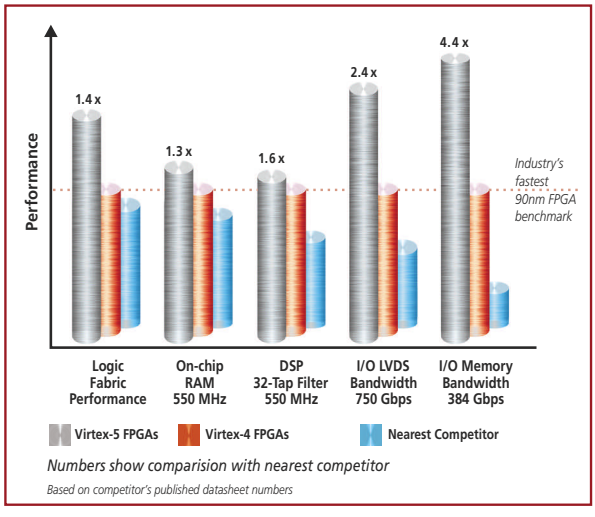

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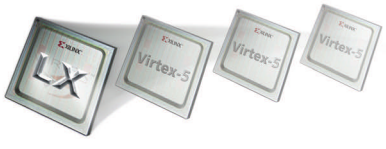

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Never stop thinking

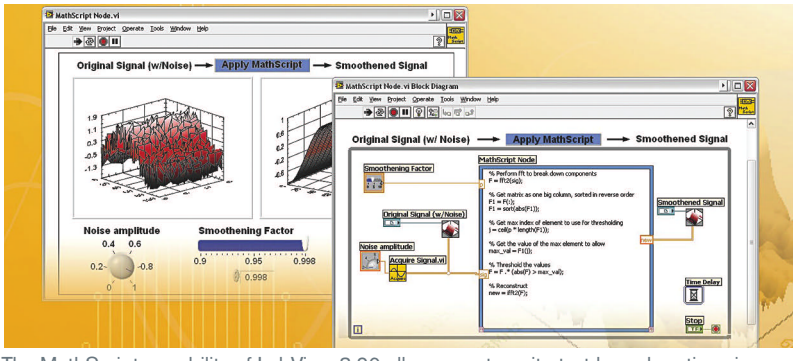
LabView celebrates 20th anniversary with new version, new features

The lifetime of successful programming languages is approximately 50 years, according to James Truchard, PhD, co-founder, chairman, and chief executive officer of National Instruments. That's an amazing amount of time in this era of product lifetimes that are typically months rather than years. NI's flagship product, LabView, an application-development environment that embodies its own graphical-programming language, is now 20 years old. In honor of that milestone, NI is announcing Version 8.20 and is looking at LabView's future path for the next 30 years. Although LabView doesn't try to be all things to all people and is not as ubiquitous as applications such as word processors and general-purpose spreadsheets, it continues to spread its wings wider to support an ever-broadening spectrum of applications in engineering and science. The software has a diverse range of capabilities and uses, most notably now including system-level EDA, embedded-system development, and FPGA-based rapid prototyping, and the user base continues its high regard for the package's ease of use.

Among the key additions to Version 8.20 is MathScript, which allows algorithm development in such text-based third-party packages as the MathWorks' (www.mathworks.com) Matlab and Comsol's (www.comsol.com) Comsol Script. Version 8.20 also supports object-oriented programming with the ability to create classes and objects; encapsulate data and methods; define methods as public, private, or protected; and more. This version also improves on LabView's control-system-development capabilities with, among other upgrades, a 14-times speed increase in execution of PID (proportional-integral-derivative) algorithms. LabView lets you take advantage of multicore CPUs, which are rapidly becoming standard in PCs. Order-of-magnitude execution-speed improvements are common when you move LabView applications from conventional processors to dual-core units. Prices for LabView start at $1199.

—by Dan Strassberg

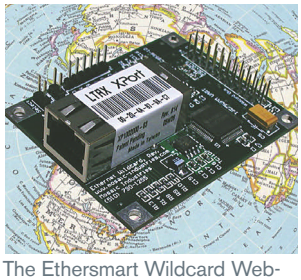
▷**National Instruments**, www.ni.com.



The MathScript capability of LabView 8.20 allows you to write text-based routines in third-party languages and incorporate the routines within LabView block diagrams.

Tiny board delivers Web connectivity

A frequent design-retrofit task is to add network connectivity to stand-alone embedded controllers or handheld instruments. Targeting these efforts, Mosaic Industries recently announced the Ethersmart Wildcard, a 2×2.5-in. expansion board that allows application programs to send e-mails, transmit data, or alert other computers on the network when significant events occur. The company based the board on the Lantronix (www.lantronix.com) Xport, which combines an x86 processor, flash memory, a 10/100-Mbit Ethernet network-interface controller, and an RJ-45 jack.



The Ethersmart Wildcard Web-enables stand-alone instrumentation to remotely monitor status, diagnose problems, or update software.

An onboard UART buffers data between the Xport and the host controller. The Ethersmart Wildcard implements multiple Web protocols to establish and manage communications. Precoded software allows applications to compose and send e-mail, establish a TCP/IP (Transfer Control Protocol/Internet Protocol) connection to exchange data, and accept connections from a Web browser to serve dynamic Web pages in response to queries. The Ethersmart Wildcard is now available and sells for $140 (100).**—by Warren Webb**

▷**Mosaic Industries Inc**, www.mosaic-industries.com.

Lithography-savvy IC router circumvents third parties

Physical-IC designers now have an alternative to Cadence (www.cadence.com), Synopsys (www.synopsys.com), and Magma (www.magma-da.com) physical-design flows: Sierra Design Automation's new detailed-router tool. The router joins the company's Pinnacle, a combination floorplanner, physical-synthesis, and clock-tree-synthesis tool. The new tool, the Olympus-SOC (system-on-chip) netlist-to-GDSII (Graphic Design System II) suite, competes directly with Cadence's Encounter, Synopsys' IC Compiler and Magma's Blast and new Talus RTL-to-GDSII suites.

Pinnacle supports multimode design, in which ICs have, for example, off, low-power, standby, and full-performance modes. It is becoming common for advanced-IC designs to have several blocks, each of which can operate in multiple modes. Thus, designers need to account for multiple combinations of mode switching. Pinnacle users can check the impact of multimode and multiprocess corners on timing, power, and signal integrity, but the availability of Olympus eliminates the need to pass that information to a third-party detailed router.

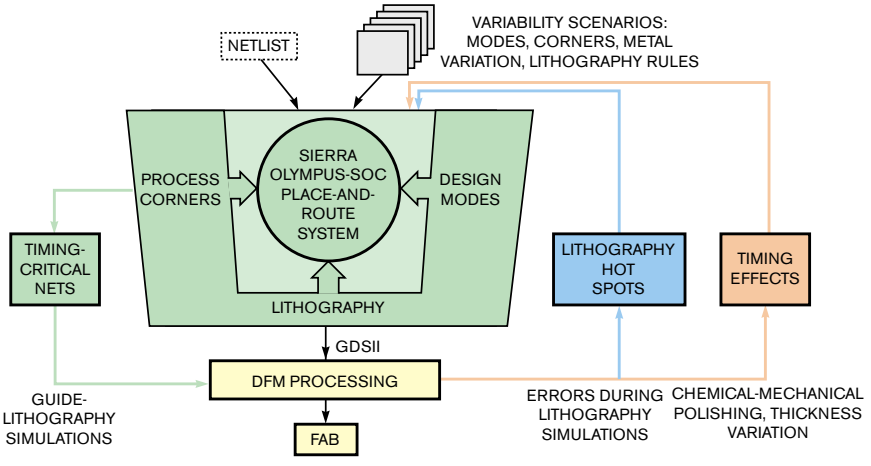
Shankar Krishnamoorthy, chief technology officer of Sierra, says that there hasn't been a significant breakthrough in routing since Magma introduced Blast about eight years ago. Routing needs have evolved, he says, and GDSII netlists now have to accurately account for not only DRC (design-rule checking), but also lithography. "We've been developing this router for the last two years and working closely with our customers' lithography groups to understand the issues they see with the layouts passed to them," says Krishnamoorthy. He notes that, whereas most DFM (design-for-manufacturing) start-ups focus on analysis or finding DFM problems, more tools are necessary to help fix the problems or to correctly implement designs in the first place. "Finding the problem is probably a quarter of the solution," says Krishnamoorthy. "At 65 and 45 nm, the number of manufacturing faults is going to be so great, you need to move into the implementation phase, so that you are producing designs that are correct by construction rather than reacting to something that is broken."

The new router is a hybrid technology that uses engines with and without grids. Krishnamoorthy says that the tool stays on the grid for most routes but directs traces off the grid to make connections to vias, for example, to avoid creating unnecessary notches that can degrade performance or cause failures in lithography. Whereas most routers target line and spacing rules, the Sierra router focuses on geometric patterns and automatically flags and fixes routing situations that are lithographically incorrect. These situations include pinching, bridging, overlap, and minimum-space and -width violations. The tool also has a DRC engine to ensure that the targeted process rules are guiding the routing, as well. The DRC engine isn't of sign-off quality, so you still need a third-party DRC/LVS (layout-versus-schematic) tool for final verification.

Users feed the Sierra Olympus-SOC system a synthesized netlist and variability scenarios describing modes, corners, on-chip variation, metal variation, and lithography rules. The tool then works with third-party critical-area-analysis, simulation, and timing tools to route the design.

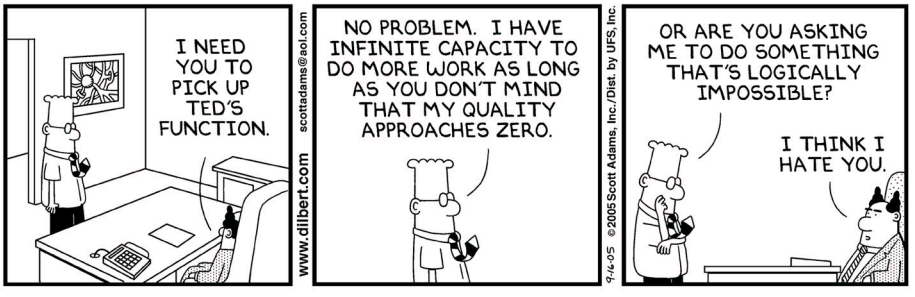
—by Michael Santarini

▷**Sierra Design Automation**, www.sierra-da.com.



The Olympus-SOC router focuses on geometric patterns and automatically flags and fixes routing situations that are lithographically incorrect.

DILBERT *By Scott Adams*



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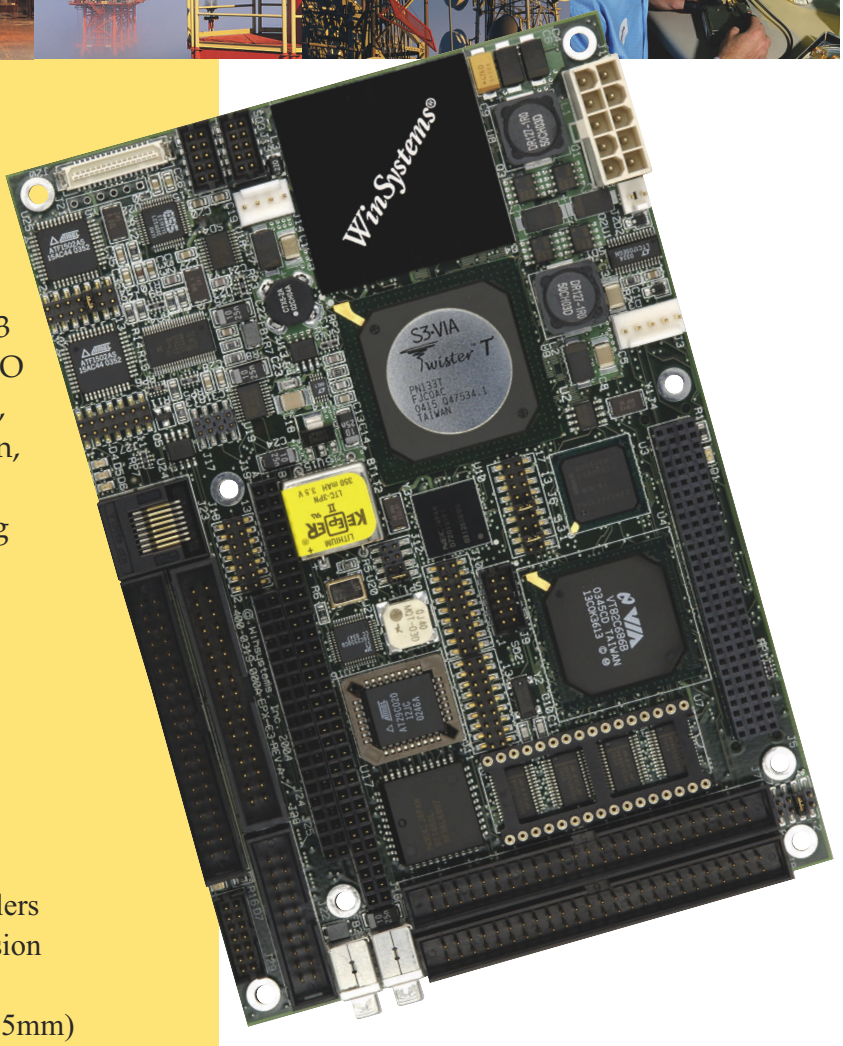

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Packet switching comes to backplanes

By looking at switching equipment, you'd never know that the trend in the communications and networking world is toward TCP/IP (Transfer Control Protocol/Internet Protocol). Once packetized data enters a line card and passes through a traffic-manager ASIC or NPU (network-processing unit), it almost universally emerges onto the backplane as fixed-length cells, rather than as packets. Such is the lingering legacy of ATM (asynchronous-transfer mode), or, if you have a longer memory, of ISDN (Integrated Services Digital Network).

Serious inefficiencies occur in the communication between variable-length packets and fixed-length cells, however. Each cell must have a header. And, as the network schedules, prioritizes, and divides packets into cells, these headers, along with the inability to fill all the cells, can lose as much as 50% of the data bandwidth, according to Robert Sturgill, president and chief executive officer of start-up Enigma Semiconductor. Sturgill may be biased, however, because Enigma has just announced an alternative approach: a family of scheduling and switching chips that moves variable-length packets across backplanes at the kinds of speeds today's metropolitan-area-network edge routers and multiservice switches demand.

> In byte-aligned transmission, nearly head-to-tail packets stream through a switching fabric.

Sturgill says that switching packets across the backplane poses formidable problems. You must concatenate packets with little dead time between them. Otherwise, the resulting efficiency is worse than for a cell-based switching system. And the shared-memory architectures for packet switching scale well only up to the limits of the memory chips for implementing those architectures.

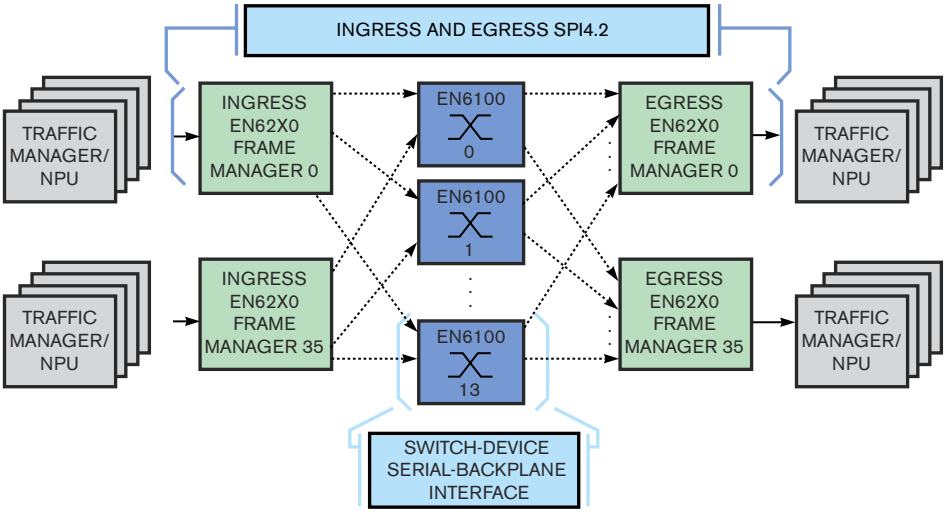
With these problems in mind, Enigma developed a fabric manager employing an algorithm that relates to SONET (synchronous-optical-network) virtual concatenation. In this approach, "byte-aligned transmission," nearly head-to-tail packets stream through a switching fabric. Combining this idea with an exhaustively tested on-the-fly scheduling algorithm and a lightweight packet header produces a system architecture that reaches 98% efficiency, according to the company's simulations. Meanwhile, the new fabric attacks the problem of scalability by abandoning the shared-memory approach, instead employing full crossbar switches. Adding switch chips linearly expands the fabric's bandwidth.

For implementation, Enigma's designers employed a two-chip approach using TSMC's 130-nm, low-voltage process. The first chip, the fabric manager, resides on the line cards and connects to four SPI 4.2 streams to and from traffic managers or NPUs. The chip prioritizes packets according to quality-of-service request tags, attaches their headers, and concatenates them into an outgoing stream toward the fabric—or vice versa for traffic moving in the other direction. The proprietary prioritization scheme provides for eight classes of service. According to Enigma's vice president of marketing, Ian Ferguson, the device can also dedicate some links to handle either switched-network traffic or video-over-Internet Protocol and similar payloads. The chip includes a significant amount of on-chip memory to eliminate the cost and space of using off-chip RAM on the line card.

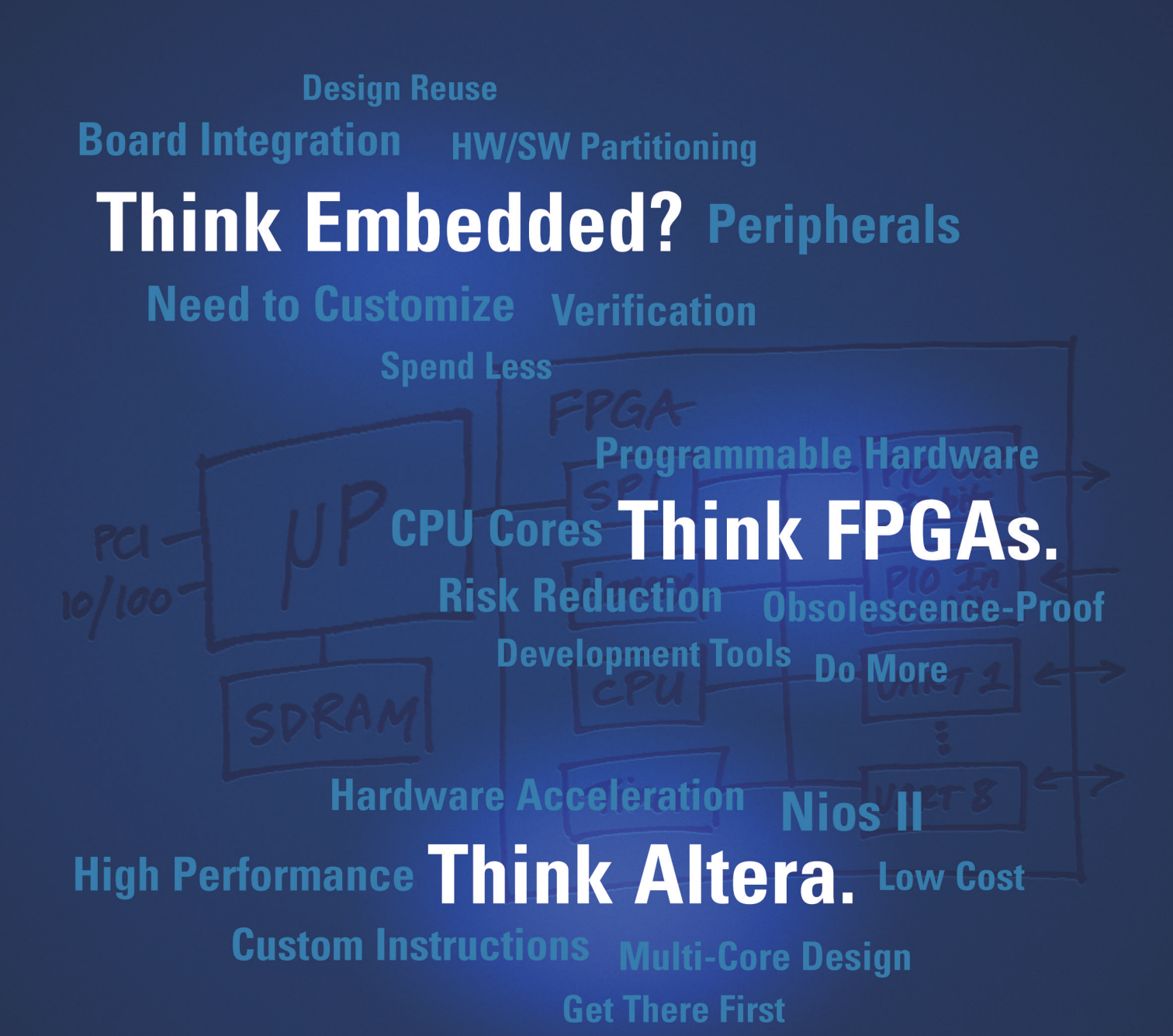
To connect the fabric manager to its fabric, Enigma employs the ABP (Advance Backplane) physical-layer technology from Rambus (www.rambus.com), allowing a speed of 12.5 Gbps per link between line cards and the backplane. The availability of a variety of codecs permits designers to choose a trade-off point for raw speed versus reliability.

The second chip, the EN-61xx crossbar switch, integrates as many as 36 ABP-links per chip and can reach an aggregate throughput of 360 Gbps of nonblocking, full-duplex traffic. The devices will be available in a range of sizes and ABP-link maximum speeds. The company expects to have both chips, the supporting system-level simulation, and the modeling tool available for sampling this month.**—by Ron Wilson**

▷**Enigma**, www.enigma.com.



Enigma's fabric manager and crossbar-switch chips schedule and switch complete packets across backplanes using links operating as fast as 12.5 Gbps.



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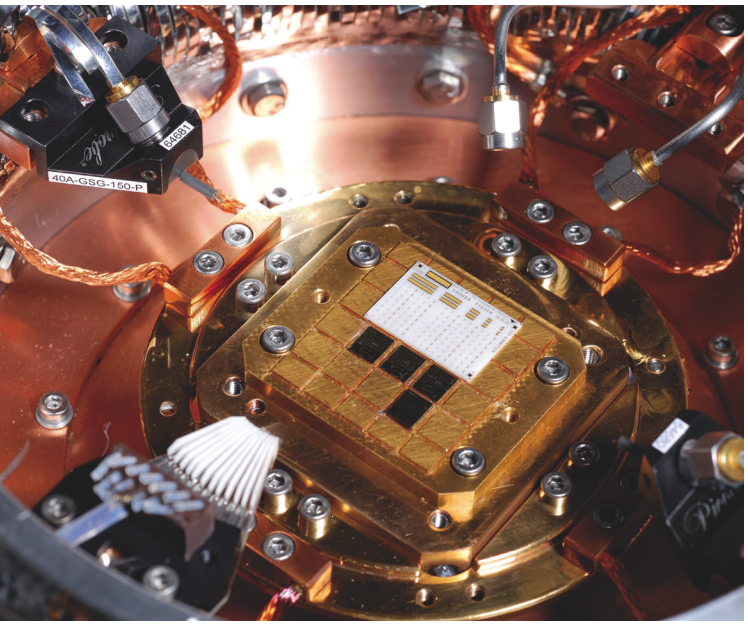

SiGe-based chips (black squares) sit inside a cryogenic test station, where they demonstrated speed of 500 GHz when cooled to 4.5K (courtesy Georgia Institute of Technology).

RESEARCH UPDATE

BY MATTHEW MILLER

Semiconductors, wireless SiGe transistors hit 500 GHz

A team of researchers from IBM and the Georgia Institute of Technology has demonstrated SiGe (silicon-germanium), heterojunction, bipolar transistors operating at more than 500 GHz. Although the group used liquid helium to cool the transistors to 4.5K (−451°F) to obtain the result, the same devices operated at 350 GHz at room temperature, and better-optimized transistors could approach terahertz room-temperature rates, according to the research team.

IBM fabricated the test devices on a prototype, fourth-generation SiGe process using 200-mm wafers and an older, nonoptimized mask set. The speed record suggests that SiGe may be able to perform beyond the performance limits scientists presume under current theory; the group's next task is to explain the physics behind the better-than-expected performance.

▷**Georgia Institute of Technology**, www.gatech.edu.

▷**IBM,** www.ibm.com.

Battery-free sensors convert motion into energy

MicroStrain has won a US Navy contract to develop wireless strain sensors that can operate indefinitely thanks to their ability to harvest energy from the rotating helicopter components on which they are installed.

The piezoelectric components generated approximately 1 mW in tests simulating straight, level flight and approximately 5 mW in simulations of maneuvers such as hard climbs and gunnery turns. The sensors, used to monitor strain for monitoring fatigue and estimating component life, consume 0.9 mW while sampling 40 times/sec and transmitting their findings as far as 70m, according to the company.

▷**MicroStrain**, www.microstrain.com.

MIT researchers built a spherical arrangement of optical fibers that senses the direction, intensity, and phase of incoming light (courtesy Greg Hren, MIT).

Components, hardware, and interconnect webs of optical fiber see in all directions

Researchers at the Massachusetts Institute of Technology have fashioned a web of optical fibers into an optical system that boasts potentially useful advantages over conventional 2-D lenses or detectors.

The 1-mm-thick fibers feature a glass core that has metal electrodes running along its length and is encased in a transparent, polymer insulator. When researchers weave these fibers into a spherical shape, they constitute an optical system that–with the help of a computer for interpretation–can detect the direction, intensity, and phase of incoming light.

Unlike conventional lenses, which are limited to the view along a certain axis, the fiber spheres can sense light all around them. The researchers cite flexibility, durability, and low weight as other advantages of the technology over conventional lenses. A densely woven fabric of smaller diameter fibers could one day enable visually aware clothing for soldiers or people with sight impairments, according to the MIT team.

▶**Massachusetts Institute of Technology**, www.mit.edu.

08.17.06

16-bit touch controller for the best user experience.
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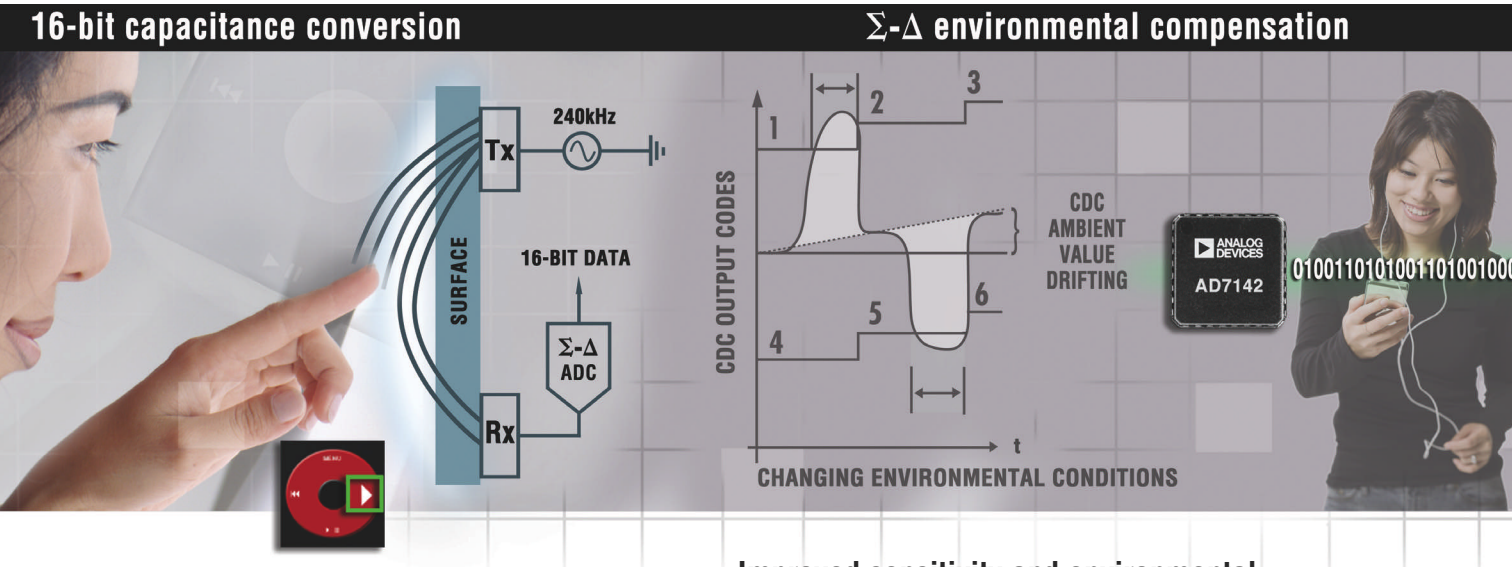

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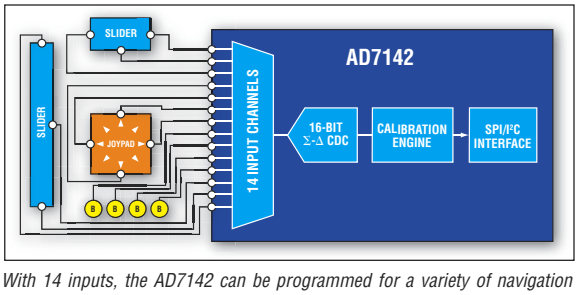

With 14 inputs, the AD7142 can be programmed for a variety of navigation functions including buttons, sliders, scroll wheels, and joypads.

Improved sensitivity and environmental calibration—made possible by Σ-Δ conversion

For products with increasing feature convergence, finger-driven navigation enhances the user experience—for designers as well as consumers. The AD7142 capacitance-to-digital converter (CDC) with on-chip environmental compensation delivers unmatched touch control performance. It offers:

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ANALOG DEVICES

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India's Innoviti connects watches to wireless data

Bangalore start-up Innoviti Embedded Solutions has developed a two-chip, wireless product that enables wrist watches to receive personalized messages and news feeds. One chip performs the RF-reception tasks, and the second controls other functions, including timekeeping, power management, and display.

The RF chip operates in the FM band of 88 to 108 MHz and uses the excess bandwidth available in commercial FM-radio-transmission streams to send data as a subcarrier. This approach enables data to coexist with the radio transmission and allows radio stations to use their infrastructure to provide value-added services. The company based the controller chip on an 8051 core, and the device has a two-cycle execution with power-efficient modes.

The main challenges in designing the product were controlling power consumption and cramming the package into a small profile to fit into a typical watch case. Because RF reception usually results in high power consumption, the designers implemented reception in time slots that synchronize with the transmitting server to cut power demand. The watch uses an OLED (organic-LED) display in place of more common LCDs to reduce power consumption. OLEDs are power-efficient and slim, and they provide high visibility, even in low-lighting conditions.

The size constraint for the design was less than 6 mm for the combined electronics, display, and battery. "One of the toughest challenges in the entire design was the antenna design. At 100 MHz, the wavelength is 3m, so an efficient antenna design would require at least 75m^3 of space," says Ashok Baragi, Innoviti's vice president of engineering. "We had to figure out how to use the watch's internal mechanical features to create an antenna."

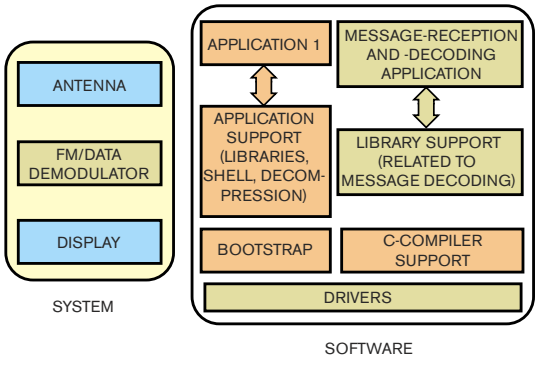
For power, the watch uses a lithium-ion battery because it provides a high capacity in a small form factor. However, watch manufacturers may switch to lithium-polymer varieties because manufacturers can fabricate them in different shapes to cater to various watch profiles.

Sophisticated built-in software enables the watch to perform its data-reception tricks. The challenge was to abstract the software architecture from the hardware interfaces to provide for easy layering—without adversely affecting power consumption. A lean core kernel with a simple scheduler manages the hardware interfaces. The scheduler synchronizes with the transmitter, which runs on an independent clock, using a network-timing reference that transmits to the receiver.

A leading watch manufacturer is currently evaluating Innoviti's design for commercialization but has not announced a schedule for public availability of a watch based on this technology.

—by Chitra Giridhar, *EDN Asia*

▷**Innoviti Embedded Solutions**, www.innoviti.com.



Innoviti's two-chip, wireless product enables wrist watches to receive personalized messages and news feeds. The design separates the software architecture from the hardware interfaces to provide for easy layering—without affecting power consumption.

> The challenge was to abstract the software architecture from the hardware interfaces.

08.17.06

Research giant, vision expert collaborate on 3-D-chip-package research

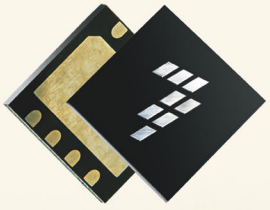
With products ranging from handsets to MP3 players to industrial-control systems shrinking in footprint, system designers must find innovative ways to package the electronics. Using 3-D IC packages is one technique that can help. For instance, cell phones often use memory stacked on top of baseband processors. Still, limited choices of 3-D techniques are currently available, so research giant IMEC (Interuniversity Microelectronics Center, Leuven, Belgium), is teaming with Icos Vision Systems in a program focusing on inspection and metrology for 3-D packaging.

Researchers will work at IMEC's laboratories, and Icos will provide technology and equipment for inspection and metrology. The joint-research program will concentrate on the development and optimization of several 3-D-packaging processes for ICs, including WLP (wafer-level packaging), flip-chip packages, SIPs (systems in packages), and MEMS (microelectromechanical systems) and on the optimization of the 3-D-metrology methods for these applications. IMEC is also hosting an affiliation program on 3-D stacked ICs, and the new program will complement that effort.

—by Maury Wright

▶**Icos Vision Systems**, www.icos.be.

▶**IMEC**, www.imec.be.



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BY HOWARD JOHNSON, PhD

Voltage-regulator model

I love switching-regulator modules. They are efficient, you can configure them for many uses, and you can easily model them.

Figure 1 shows a typical characterization test for a regulator module—a Texas Instruments PTH08T220W switching-regulator module. The module is subject to an 8A step load, with a maximum dI/dt of 2.5V/µsec. The plot shows the load current at the bottom and the voltage-regulator response to this current at the top.

To build a circuit model for this voltage regulator, you need no additional information about the insides of the regulator. The step-response test reveals enough information to form a simple circuit model (**Figure 2**). The circuit model assumes a perfect voltage source, V_{REF}, connected through components R_1 and L_1 to your V_{CC} plane. Components R_1 and L_1 represent the action of the regulator.

Component C_2, along with R_2 and L_2, represent the bulk capacitor (or array of bulk capacitors) in your application.

If, by looking at the data sheet, you can discover values for R_1 and L_1, then you can build a circuit model such as the one in **Figure 2** for any application of the regulator.

The most straightforward parameter in this circuit is R_1. Over a time period of more than 100 µsec, the circuit comes to rest at a steady-state dc operating condition. After that time, capacitor C_2 draws no appreciable steady-state current, so you may replace it with an open circuit. Similarly, replace inductor L_1 with its dc equivalent: a short. The only operative component remaining in the circuit is resistor R_1, which directly controls the output droop, or steady-state dc offset. The value of R_1 equals the ratio of droop to load current.

Over a medium scale of time, components C_2 and L_1 come into play, creating a damped sinusoidal response. The application note for this component shows a typical step-response waveform with 1200 µF of output capacitance. Given that data point, you just set C_2 equal to 1200 µF and adjust L_1 to match the width of the sinusoidal glitch. Now you know L_1!

Last, given R_1, C_2, and L_1, adjust R_2 until you match the damping factor of each sinusoidal pulse. Now you know what ESR (equivalent series resistance) that manufacturer used when it snapped the step-response picture.

This simple circuit mimics the performance of the regulator at frequencies from dc to approximately 100 KHz. Above that range, the ESL (equivalent series inductance) of capacitor C_2 comes into play, but this low-speed step-response test doesn't provide enough information to determine L_2. For a low-speed model, just leave L_2 at zero.

This simple circuit model works for any voltage regulator with dominant-pole feedback, meaning that the regulator does not use a multipole phase-compensating feedback structure. (Most don't.)

Always follow the manufacturer's guidelines for minimum capacitance and minimum ESR in your output capacitors. Failure to do so can produce unstable oscillations in the feedback circuit, destroying your circuit. **Figure 2** does *not* model that aspect of regulator behavior.EDN

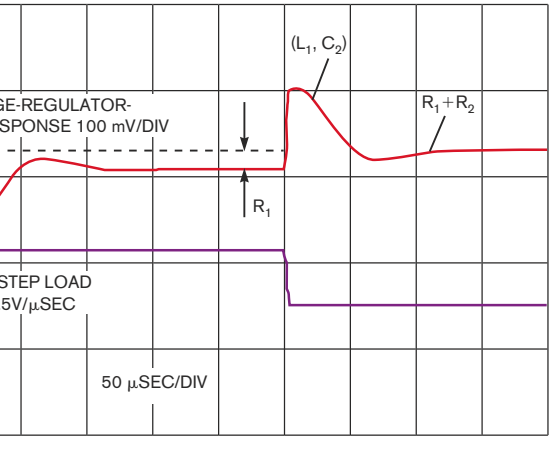

Figure 1 Four parameters control the low-frequency step response.

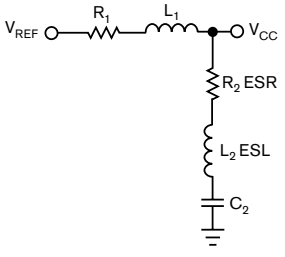

Figure 2 Most voltage regulators behave like this simple circuit.

Howard Johnson, PhD, of Signal Consulting, frequently conducts technical workshops for digital engineers at Oxford University and other sites worldwide. Visit his Web site at www.sigcon.com or e-mail him at howie03@sigcon.com.

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HP-IB revolutionized ATE: Designers benefited from smarter connected instruments

The article that Hewlett-Packard contributed to *EDN* in 1972 describing an instrumentation bus didn't even mention HP-IB (Hewlett-Packard Instrument Bus). But, as the photo confirms, the article was the clear precursor to the HP-IB interface that competitors later dubbed the GPIB (General Purpose Interface Bus) and that ultimately became the IEEE-488 interface. HP defined the bus both to allow instruments to communicate among themselves and to host computers or even calculators. Read the complete archived article on our Web site, and you'll find that the developers of the bus realized how valuable data dumps to a computer could be and how important the specification of a standard communication protocol would be in addition to the standardized physical interface.

The IEEE-488 interface became ubiquitous in the test-and-measurement industry by the late 1970s. HP and others even used the interface to connect computer peripherals, such as disk drives and monitors. Although the ATE (automatic-test-equipment) segment may have been the biggest beneficiary of the bus, design engineers also gained more capable and intelligent instruments largely due to the prolific IEEE-488 standard.

The interface was also a precursor to backplane-centric test systems, such as PXI (PCI extensions for instrumentation), and even to the trend toward virtual instruments based largely on Intel-processor-based PCs. Engineers still widely use the IEEE-488 bus, although it is giving way in many applications to technologies such as PXI and virtual instruments. But the IEEE-488 concept may live a lot longer, because an industry group is developing the LXI (LAN-extensions-for-instrumentation) standard to move to an Ethernet-based alternative. EDN

09.01.72

FROM THE VAULT

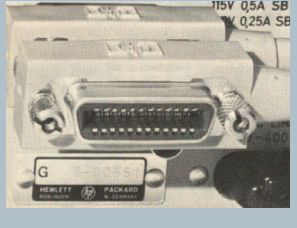
Digital bus simplifies instrument-system communication

INTERCONNECTING PROGRAMMABLE INSTRUMENTS INTO A TEST SYSTEM IS A FORMIDABLE TASK. HERE'S A RUNDOWN ON THE CONSIDERATIONS INVOLVED, AND A BUSING SCHEME THAT DOES THE JOB.

Donald C Loughry, Hewlett-Packard Co

Effective communication between two instruments, as in human communication, requires two essential elements—a good talker and a good listener. The design and use of instrumentation systems usually require many such communication links, or interfaces, as commonly termed. The practical implementation of these interfaces is not always easy.

Recognition of the fact that interface design involves much more than visible elements of cables, connectors, and circuits in the exchange of digital messages between instruments is of critical importance. All too often it is assumed that agreement on physical-hardware requirements will achieve compatibility. Circuit compatibility, perhaps, but that is only part of the picture. The scope of the messages to be communicated, the unambiguous definition of message content, and the techniques for exchanging these messages within a communications network are all important. Factors such as codes, formats, control techniques, timing, logic conventions and software requirements cannot be overlooked. Effective communications via a digital-interface system must consider all of these parameters. What then are some of the specific problem areas causing outright incompatibility or, at best, costly interface design?



MESSAGE TRAFFIC INCREASES: A few years ago, only the most frequently changed and easily programmed front-panel controls were candidates for remote control. Now, it is not unusual to have all the front-panel controls on an instrument available for digital remote program control, even those usually implemented by analog means, such as vernier controls.

STORAGE: Although the scene is changing, many products still do not contain storage capability on program-data input or basic-data output lines. The absence of storage places extra demands on the interface as well as on some of the system elements.

MESSAGE CONVENTION: Each digital message carried on the interface must have an assertion state or logic convention associated with it. This is no different than many other conventions in life. Who would want to drive on the right-hand side of the road in the UK?

The need for automatic measurements coupled with the availability of low-cost digital-device technology to do the job have reduced the interface problem significantly. What used to take literally tens of interface interconnections all demanding new input data throughout a measurement cycle now requires but a few lines providing data input much less frequently. The result: Smart instruments are now able to communicate in a higher-level language, simplifying the interface task.—*EDN*, Sept 1, 1972

ANALOG edge℠
Expert tips, tricks, and techniques for analog designs
Vol. IV, Issue 7
DESIGN idea

Improving Video Clock Generation in Modern Broadcast Video Systems

By Alan Ocampo, Applications Engineer

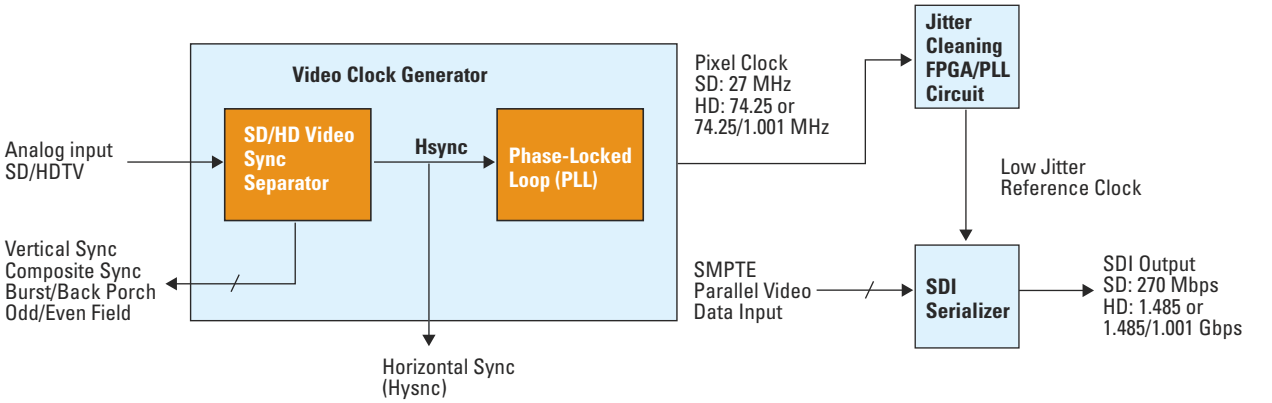


Figure 1. SDI Reference Clock Generator Block Diagram

The old adage "timing is everything" is well embodied in the modern broadcast studio, where precise timing of video clock and synchronization signals are essential to create, acquire, edit, and distribute analog and digital video. Today's broadcast systems must support industry-standard SD/HD formats, such as NTSC, PAL, 720p, 1080i, and 1080p, over analog and digital interfaces such as composite, component, and Serial Digital Interface (SDI). With high-speed SDI video equipment being increasingly used throughout the studio, improved video sync separation can more effectively produce video clocks with low jitter, which is crucial to meeting the stringent specifications of new SDI standards.

A video clock generator which generates various timing and clock signals from an analog video input consists of a video sync separator and Phase-Locked Loop (PLL). These two circuits are illustrated in the SDI application block diagram in *Figure 1*.

The video sync separator accepts a $1V_{p-p}$ analog video input with bi-level or tri-level sync and extracts the standard timing signals, such as Horizontal (Hsync), vertical, and composite sync, burst/back porch, and odd/even field outputs. To meet strict timing requirements of the latest HDTV standards, specifications such as HD tri-level sync separation, low output propagation delay, and 50% sync slicing are imperative. The latter ensures precise sync extraction by slicing at the proper 50% point of the bi-level or tri-level sync reference edges. This provides for improved Hsync jitter performance compared to non-adaptive, fixed-level sync slicing, even under irregular input conditions such as double or no 75Ω load termination or transmission loss. Hsync jitter is defined here as the peak-to-peak time variance in Hsync's falling-edge with respect to the input's sync reference-edge and is critical to the performance of the pixel clocks generated by the subsequent PLL block.

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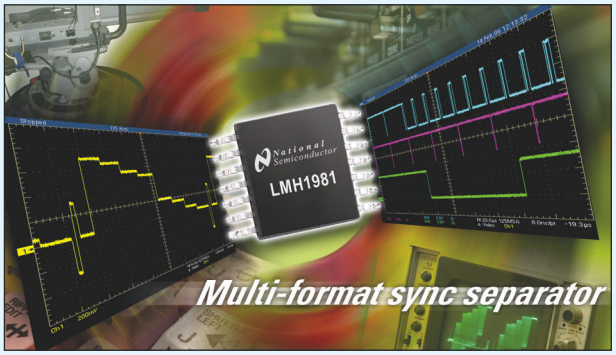
Featured Products

Multi-Format Video Sync Separator

The LMH1981 is a multi-format sync separator for high-definition broadcast and professional video systems. The device automatically detects the input video format and performs all the necessary sync separation to generate low-jitter horizontal and vertical sync signals for standard and high-definition video formats, including NTSC, PAL, SECAM, 480i, 480p, 576i, 576p, 720p, 1080i, and 1080p.

The LMH1981 features the timing outputs needed for any video system, including horizontal, vertical and composite sync, odd/even field, burst/back porch clamp, and a patented automatic video-format detection feature. The device accepts both bi- and tri-level sync video inputs and features 50% slicing to ensure accurate separation of signals that vary in amplitude, offset, and noise. The device has a wide input range, allowing the inputs to accept video signals from 500 mV_{P-P} to 2 V_{P-P}.



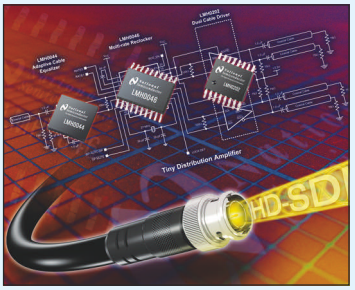
Features

- 50% sync slicing
- Low jitter horizontal sync output
- Supports NTSC, PAL, SECAM, 480i, 480p, 576i, 576p, 720p, 1080i, and 1080p
- Accepts video signals from 500 mV_{P-P} to 2 V_{P-P}
- No external programming with µC required
- Horizontal sync output propagation delay <50 ns

The LMH1981 is ideal for use in a wide range of video applications such as, broadcast video equipment, video distribution, DTV and HDTV systems, and is available in TSSOP-14 packaging.

For FREE samples, datasheets, and more, visit
www.national.com/pf/LM/LMH1981.html

Adaptive Cable Equalizer



The LMH0044 adaptive cable equalizer is a monolithic integrated circuit for equalizing data transmitted over cable (or any media with similar dispersive loss characteristics). The equalizer operates over a wide range of data rates from 143 Mbps to 1.485 Gbps and supports SMPTE 292M, SMPTE 344M, and SMPTE 259M. This device implements DC restoration to correctly handle pathological data conditions (DC restoration may be bypassed for low data rate applications). The equalizer may be driven in either a single-ended or differential configuration.

Additional features include separate carrier detect and output mute pins which may be tied together to mute the output when no signal is present. A programmable mute reference is provided to mute the output at a selectable level of signal degradation.

Features

- SMPTE 292M, SMPTE 344M, and SMPTE 259M compliant
- High data rates: 143 Mbps to 1.485 Gbps
- Equalizes up to 200m of Belden 1694A at 1.485 Gbps or up to 400m of Belden 1694A at 270 Mbps
- 208 mW typical power consumption with 3.3V supply
- Manual bypass and output mute with a programmable threshold
- Single-ended or differential input
- Supports DVB-ASI at 270 Mbps
- 50Ω differential outputs
- Single 3.3V supply operation

The LMH0044 is ideal for SMPTE 292M/344M/259M serial interfaces, serial digital data equalization and reception, and data recovery equalization. The LMH0044 is available in LLP-16 packaging.

For FREE samples, datasheets, and more, visit
www.national.com/pf/LM/LMH0044.html

Improving Video Clock Generation in Modern Broadcast Video Systems

The PLL block can generate one or more pixel clocks, which should be phase-locked to the leading-edge of Hsync, the PLL's reference input. To produce both SD and HD pixel clocks will require two PLLs, both designed to give the appropriate output frequency for any given Hsync frequency. Since the PLL derives a higher frequency pixel clock from a lower frequency Hsync, pixel clock jitter will be determined by different sources at different frequencies. Below the loop bandwidth, the clock jitter output by the PLL will be dominated by Hsync jitter, which can be a significant amount depending on the performance and quality of the sync separator. Above the loop bandwidth, it will be dominated by its PLL oscillator, typically a Voltage-Controlled Crystal Oscillator (VCXO) chosen properly for low phase noise and frequency tuning, among other characteristics.

In the block diagram, a pixel clock generator is used to derive a reference clock for an SDI serializer which receives SMPTE-compliant parallel digital video data and then encodes, serializes, and transmits uncompressed serial digital video over coax cable. A serializer requires a clean reference clock for its internal PLL to generate a bit rate clock that maintains the serializer and clocks its output bit-stream. If used to directly clock the serializer, any jitter on the reference clock could potentially transfer to the bit rate clock and consequently appear as SDI output jitter. As shown in ***Table 1***, SDI formats use increasingly high data rates and thus require clock sources with sufficient jitter performance.

For example, SMPTE 292M specifies the "timing" and "alignment" jitter requirements for an HD-SDI serializer's output bit-stream. Referring to the table, timing jitter should not be more than 1.0 UI[1] for jitter frequency components from B1 to B3, or 10 Hz to 1485 MHz, per SMPTE 292M. Alignment jitter—which is the high-frequency subset of timing jitter—should be no more than 0.2 UI from B2 (100 kHz) to B3. Outside of their respective frequency limits, both the timing and alignment jitter specifications roll off at 20 dB per decade. Output jitter above the jitter specifications can result in degradation of error performance at the SDI deserializer. Please see the SDI standards for more information.

The stringent jitter specifications of SDI standards demonstrate the profound need for a low-jitter pixel clock. In most cases, however, a generated pixel clock will have an intolerable amount of jitter, up to 6 ns_{p-p} for a typical SD pixel clock, which precludes direct application as a reference clock. Jitter reduction is therefore required to improve such unacceptable clock performance. The most common way to reduce pixel clock jitter is to use jitter-cleaning circuitry, usually implemented with additional Field-Programmable Gate Array (FPGA) or PLL stages. While jitter-cleaning circuitry is routinely applied by system designers, this can add significantly to component count, PCB area, power, and design cost and time.

A more effective way to reduce pixel clock jitter and thus improve SDI output jitter is to use a broadcast-quality video sync separator that has very low Hsync jitter, such as the LMH1981. This improved performance gives designers the flexibility to use smaller FPGAs or otherwise reduce jitter-cleaning circuitry and still produce an SDI output that complies to the jitter specifications.

Although broadcast systems are rapidly transitioning to high-speed SDI formats, the need to generate accurate video clocks from analog sources to process digital video data will be around for years to come. Current solutions require extensive jitter-cleaning circuits for generating an accurate reference clock to produce a SMPTE-compliant SDI output. However, the most fundamental and effective solution is to minimize jitter on the most critical timing reference, Hsync. This can only be accomplished using a high-performance analog video sync separator such as the LMH1981 in the clock generation signal path because, as we now know, timing is everything. ■

Access interactive broadcast video solutions diagrams at solutions.national.com

Table 1

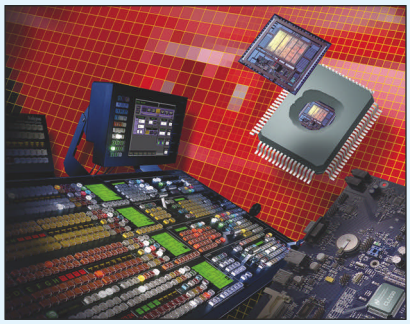
Format	Standard	Bit Rate	Output Timing Jitter (B1 to B3)*	Output Alignment Jitter (B2 to B3)*
SD-SDI Standard- definition	SMPTE 259M, 334M	270 Mbps, others not widely used	1.0 UI[1] or 3.7 ns_{p-p}	0.2 UI or 740 ps_{p-p}
HD-SDI High-Definition; HD/SD-SDI Mulit-rate	SMPTE 292M	1.485 Gbps 1.485/1.001 Gbps	1.0 UI or 673 ps_{p-p}	0.2 UI or 135 ps_{p-p}
3-Gbps SDI up to 1080p/60 over a single link	SMPTE 424M	2.970 Gbps 2.970/1.001 Gbps	2.0 UI or 673 ps_{p-p}	0.3 UI maximum, 0.2 UI recommended

*B1, B2, and B3 are the jitter frequency band limits specified in the SMPTE standards.
[1]One UI, or Unit Interval, is equal to one bit period (1/bit rate) of the serial bit-stream.

Featured Products

Digital Video Serializer with Ancilliary Data FIFO and Integrated Cable Driver

The LMH0030 is a monolithic integrated circuit that encodes, serializes, and transmits bit-parallel digital video data. The serial data clock frequency is internally generated and requires no external frequency setting, trimming, or filtering components. The LMH0030 performs functions which include: parallel-to-serial data conversion, SMPTE standard data encoding, NRZ to NRZI data format conversion, serial data clock generation and encoding with the serial data, automatic video rate and format detection, ancillary data packet management and insertion, and serial data output driving.



Features

- SDTV/HDTV serial digital video standard compliant
- Supports 270 Mbps, 360 Mbps, 540 Mbps, 1.4835 Gbps, and 1.485 Gbps SDV data rates with auto-detection
- Low output jitter: 85 ps (typ), 125 ps (max)
- Low power consumption: 430 mW (typ) from 3.3V
- No external VCO required
- Fast PLL lock time: < 150 µs (typ) at 1.485 Gbps
- LVCMOS compatible data and control inputs and outputs
- 75Ω ECL-compatible, differential, serial cable-driver outputs
- 3.3V I/O power supply and 2.5V logic power supply operation

The LMH0030 SDTV/HDTV serial-to-parallel digital video interfaces for video cameras, VTRs, telecines, digital video routers and switchers, digital video processing and editing equipment, video test pattern generators and digital video test equipment, and video signal generators. The LMH0030 is available in TQFP-64 packaging.

For FREE samples, datasheets, and more, visit
www.national.com/pf/LM/LMH0030.html

Digital Video Deserializer / Descrambler with Video and Ancillary Data FIFOs

The LMH0031 is a monolithic integrated circuit that deserializes and decodes SMPTE 292M, 1.485 Gbps (or 1.483 Gbps) serial component video data, to 20-bit parallel data with a synchronized parallel word-rate clock. It also deserializes and decodes SMPTE 259M, 270 Mbps, 360 Mbps, and SMPTE 344M (proposed) 540 Mbps serial component video data, to 10-bit parallel data. Functions performed by the LMH0031 include clock/data recovery from the serial data, serial-to-parallel data conversion, SMPTE standard data decoding, NRZI-to-NRZ conversion, parallel data clock generation, word framing, CRC and EDH data checking and handling, Ancillary Data extraction, and automatic video format determination.

Features

- SDTV/HDTV serial digital video standard compliant
- Supports 270 Mbps, 360 Mbps, 540 Mbps, 1.483 Gbps, and 1.485 Gbps serial video data rates with auto-detection
- Low power: 850 mW (typ)
- Uses 27 MHz crystal or clock oscillator reference
- Fast VCO lock time: < 500 µs at 1.485 Gbps
- Built-in self-test and video test pattern generator
- LVDS and ECL-compatible, differential, serial inputs
- 3.3V I/O power supply and 2.5V logic power supply operation

The LMH0031 SDTV/HDTV serial-to-parallel digital video interfaces for video editing equipment, VTRs, standard converters, digital video routers and switchers, digital video processing and editing equipment, video test pattern generators and digital video test equipment, and video signal generators. Operating over the commercial temperature range (0°C to +70°C), the LMH0031 is available in TQFP-64 packaging.

For FREE samples, datasheets, and more, visit
www.national.com/pf/LM/LMH0031.html

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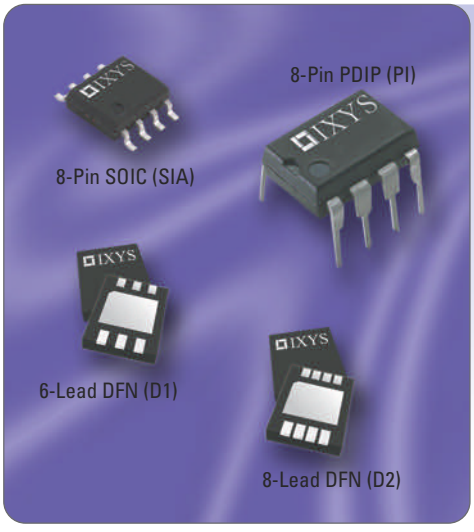
Low-Side Gate Driver ICs from 2A to 14A

Next Generation IXD_5XX Low-Side Gate Drivers With Improved Cost-Efficiency, Circuit Density and Ruggedness for MOSFETs and IGBTs



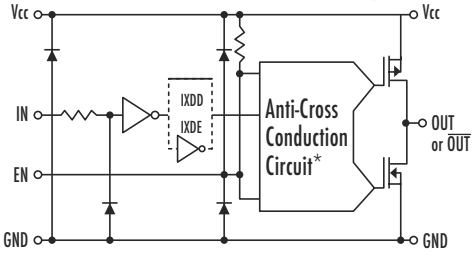
Features

- Diverse choice of single and dual outputs, with extensive mix of logic, packaging and output currents
- Enable options for fast, controlled shutdown
- Rated for operation from 4.5V to 35V and -55°C to +125°C
- Multiple packaging options, including high density 6-Lead DFN and 8-Lead DFN (4mm x 5mm)
- No internal cross conduction, output rise and fall times of 25ns maximum

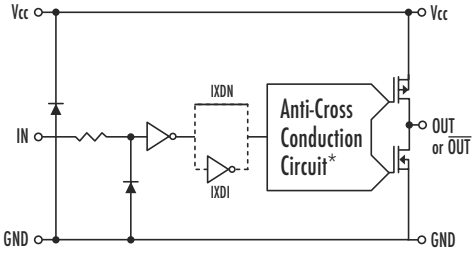
Applications

- Industrial – Inverters, Motor Drives, Welding
- Consumer – LCD TV, Audio Amplifiers
- Power Conversion – SMPS, UPS, PFC
- Actuators – Relays, Solenoids

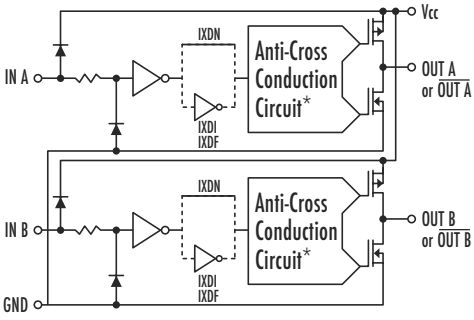
IXD(D,E)509, IXD(D,E)514 Block Diagram



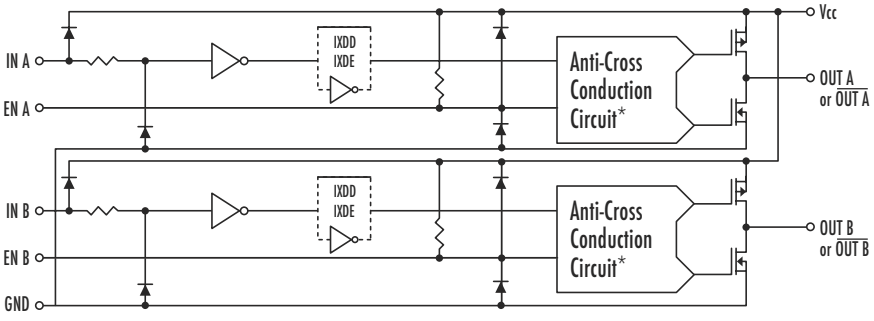
IXD(I,N)509, IXD(I,N)514 Block Diagram



IXD(F,I,N)502, IXD(F,I,N)504 Block Diagram



IXD(D,E)504 Block Diagram



Summary Tables for IDX_5XX Low-Side Gate Driver Family

Part Numbers and Configurations

Part Number	I_{PK} @ T_C = 25°C	Logic Configuration(1)	Package(2)
IXD(1)502(2)	2 A, Dual	F, I, N	PI, SIA, SIAT/R, D1, D1T/R
IXD(1)504(2)	4 A, Dual	F, I, N	PI, SIA, SIAT/R, D1, D1T/R
IXD(1)504(2)	4 A, Dual	D, E	PI, SIA, SIAT/R, D2, D2T/R
IXD(1)509(2)	9 A, Single	D, E, I, N	PI, SIA, SIAT/R, D1, D1T/R
IXD(1)514(2)	14 A, Single	D, E, I, N	PI, SIA, SIAT/R, D1, D1T/R

Logic Configurations

Designation	Configuration	Designation	Configuration
D	Non-Inverting + Enable	I	Inverting
E	Inverting + Enable	N	Non-Inverting
F	Non-Inverting and Inverting		

Package Details

Designation	Package	Packing Style	Pack Qty
PI	8-Pin PDIP	Tube	50
SIA	8-Pin SOIC	Tube	94
SIAT/R	8-Pin SOIC	13" Tape and Reel	2500
D1	6-Lead DFN	Bulk	1500
D1T/R	6-Lead DFN	13" Tape and Reel	2500
D2	8-Lead DFN	Bulk	1500
D2T/R	8-Lead DFN	13" Tape and Reel	2500

** United States Patent 6,917,227*

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Efficiency Through Technology

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Specs: Sometimes timing really *is* everything.

DANIEL VASCONCELLOS

Most of *EDN*'s "Tales from the Cube" tell a story about how a design or applications engineer encountered an unexpected technical challenge and overcame it with a clever fix. Here's a cautionary tale about how to avoid getting into trouble in the first place. The moral of the story boils down to: Be careful if you rely on device performance that you've merely observed and not specified.

The story begins when Tim Regan, a signal-conditioning-applications manager for Linear Technology, receives a call from a customer who designs and manufactures automated faucets that turn on when a hand is under the spigot and off when the hand goes away. The electronics comprise an infrared LED that pulses 100 mA for 50 µsec, 10 times a second. The circuit looks for an echo back, indicating that a hand is ready for washing.

Few plumbing fixtures come with access to ac power, so the faucets must be self-contained, relying on four AA batteries for power. The faucets need to go 15 to 20 years on one set of batteries, thus making them maintenance-free; the assumption is that the restroom will undergo remodeling before the batteries wear out. A long life is important to plumbing products, because nobody wants to hire an expensive plumber just to change batteries.

The design uses an LT1637 micropower amplifier that, when you disable it, draws only 3 µA. To conserve power, the circuit enables the amplifier for only about 25 µsec during the 50-µsec pulse; so the amplifier sets the 100-mA pulse for only about 25 µsec. However, when you enable the amplifier, it doesn't turn on immediately—there's an unspecified lag time from when the enable pin goes low to when the amplifier turns on. This delay occurs because the amplifier's power-miserly architecture is oriented toward quickly turning off the amplifier: An internal transistor has to turn off when you apply the enable-pin voltage. However, the transistor employs no pulldown resistors, because they would eat power. Rather, the base of the transistor floats down, and the speed at which it turns off depends on leakage currents at the base and by the transistor beta, which varies from wafer to wafer. A lengthy enable time shortens the IR pulse width and impairs the effectiveness of the hand sensing.

Regan explains, "Beta variation in parts is perfectly normal. A snappy turn-on of a slow, micropower amplifier is really a 'don't care' in most applications and therefore something we don't specify or monitor in production. It's something you wouldn't ordinarily think could have such a significant impact." Regan ran some studies and was able to give the customer an enable-turn-on time of 10 to 150 µsec—a wide range. Simply applying power for the entire range would have shrunk the potential battery life from more than 21 years to less than five!

The customer rethought the problem, because he now knew he couldn't rely on unspecified timing characteristics. He turned on the amplifier-enable pin for the longer, 150-µsec worst-case turn-on time, which requires about 200 µA, then pulsed the LED driver for the 25 µsec required to produce the 100-mA IR pulse. Again, Regan ran the numbers and discovered that the increase in current drain with the extended amplifier on-time lost only about 83 days of battery life. This small change resulted in a reliable design that preserved almost 15 years of battery life.

Epilogue: Regan notes that, since he worked with that customer, Linear Technology has introduced the LT6000 amplifier family, which operates with as little as 1 µA of supply current. In a faucet design, the amplifiers could remain continuously on without significant drain on the batteries. EDN

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We need a regular supply of "Tales," and who better than our loyal readers to supply them? Send a narrative describing a sticky engineering problem that bedeviled you to Maury Wright at mgwright@edn.com. If we publish your submission, we'll send you a $200 American Express gift check.

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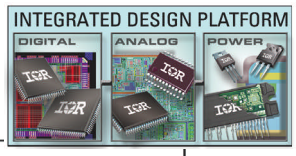

DIGITAL

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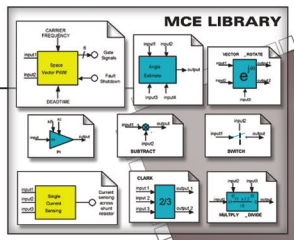
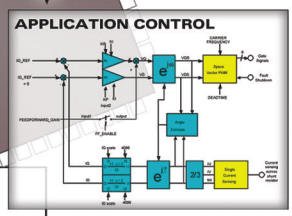
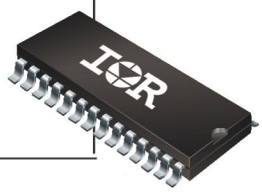




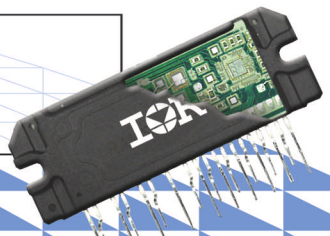
ANALOG

- Enables single DC line configuration on low-side IGBTs for current sensing
- Integrated over-current, under-voltage and cross-conduction protection

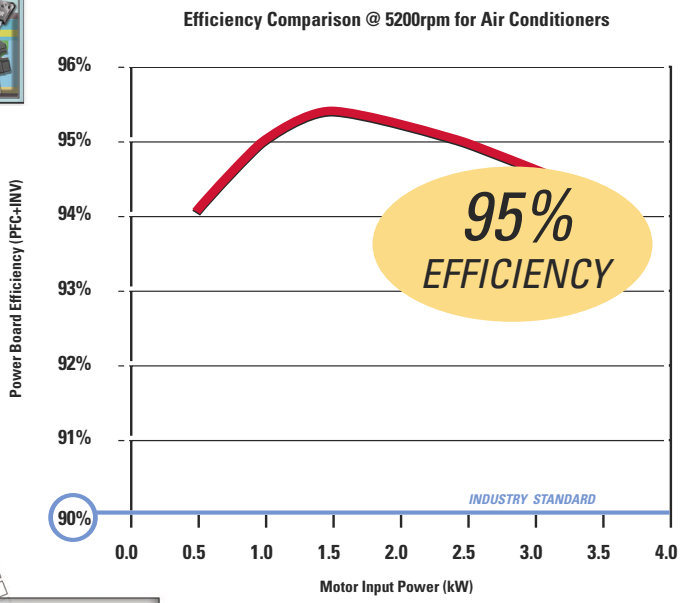


POWER

- Efficient, depletion-stop trench IGBTs
- Discrete and IPM packages



LEAD FREE



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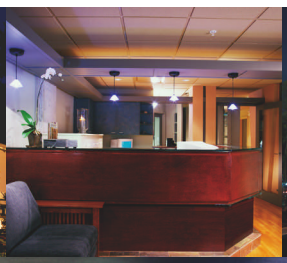
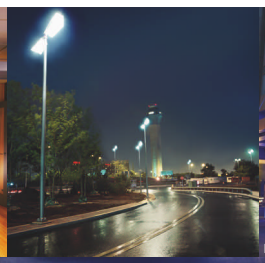

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BY WARREN WEBB • TECHNICAL EDITOR

SMART-BUILDING SYSTEMS CONVERGE

AS BUILDING-AUTOMATION DATA FLOWS ONTO ENTERPRISE NETWORKS AND THE INTERNET, DESIGNERS ARE TURNING TO INTEGRATED SYSTEMS AND WEB-BASED SERVICES.

Growing customer demands for open, interoperable subsystems, along with widely available, high-speed information-technology networks, have fueled the transformation of the building-automation sector from independent, mostly proprietary product suppliers into a standards-based industry. As this makeover progresses, building systems such as lighting, environmental, and security can share digital information with each other and with enterprise or Web-based business applications to reduce costs and respond to real-time events. In the future, you can expect smart-building technology that enables multiple structures to automatically respond to adverse weather conditions, energy shortages, nearby fires, or local crime events.

Most smart-building systems comprise a series of distributed sensors and specialized actuators connected to application software running on a local or remote processor. These systems usually have a singular building-automation purpose, such as climate control, security, or fire protection. However, as building systems become more integrated and sophisticated, control algorithms can optimize their objectives with data from external sources, such as other building subsystems, historical data, weather forecasts, and real-time energy pricing.

A major hurdle in the transition to integrated systems is the hodgepodge of communications and networking schemes that building-automation manufacturers traditionally use. Many current building subsystems communicate with standard protocols such as LonWorks (local-operating network) and BACnet (building-automation and -control network) in addition to numerous propri-

AT A GLANCE

- Smart-building systems actively exchange information to provide a productive environment for occupants at the lowest possible cost.
- Wireless networks and enterprise-information-technology cabling permit building systems to share data without new wiring.
- Low-power, low-data-rate wireless networks give smart-building systems distributed-sensor nodes to optimize control algorithms.
- XML and Web-services technology provide a common communications channel between incompatible, automatic building systems.

etary schemes. These systems require dedicated wiring between sensors, actuators, and processing elements. Now, with enterprise information-technology networks available in almost all commercial structures, building-automation designers are adapting their subsystems to take advantage of this high-bandwidth datapath. Although designers have adapted some of the building-automation protocols to exchange data with TCP/IP (Transfer Control Protocol/Internet Protocol) networks, many require special gateway devices to extract system-specific information.

BUILDING NETS

BACnet, a widely deployed, open-protocol communication standard for building systems, represents data as objects, properties, and services. This standard method of representing data and actions enables devices from different manufacturers to interoperate, although most BACnet devices are limited to the HVAC (heating, ventilating, and air-conditioning) industry. The BACnet standard defines several PHY (physical) layers, including Ethernet, BACnet/IP, and point-to-point over RS-232. BACnet is an ANSI and ISO standard that the ASHRAE (American Society of Heating, Refrigeration, and Air-Conditioning Engineers) maintains.

LonWorks, another popular building-control-system protocol, requires a proprietary Neuron chip or licensed intellectual property from Echelon Corp in each controller. The lighting, utilities, and transportation industries use the low-bandwidth LonWorks protocol, and it has more automated building installations than BACnet. The LonWorks protocol provides a set of services that allows device-application software to send and receive messages over the network without needing to know the topology of the network or the names, addresses, or functions of other devices. An open version of the protocol, ANSI/EIA709, describes the algorithm in sufficient detail to enable operation on a variety of general-purpose processors.

Although TCP/IP is a logical choice for intelligent-building architecture, many systems require a large number of sensors in areas that enterprise networks do not serve. These situations favor networking schemes—such as wireless links, power-line communications, and even telephone-line sharing—that do not require

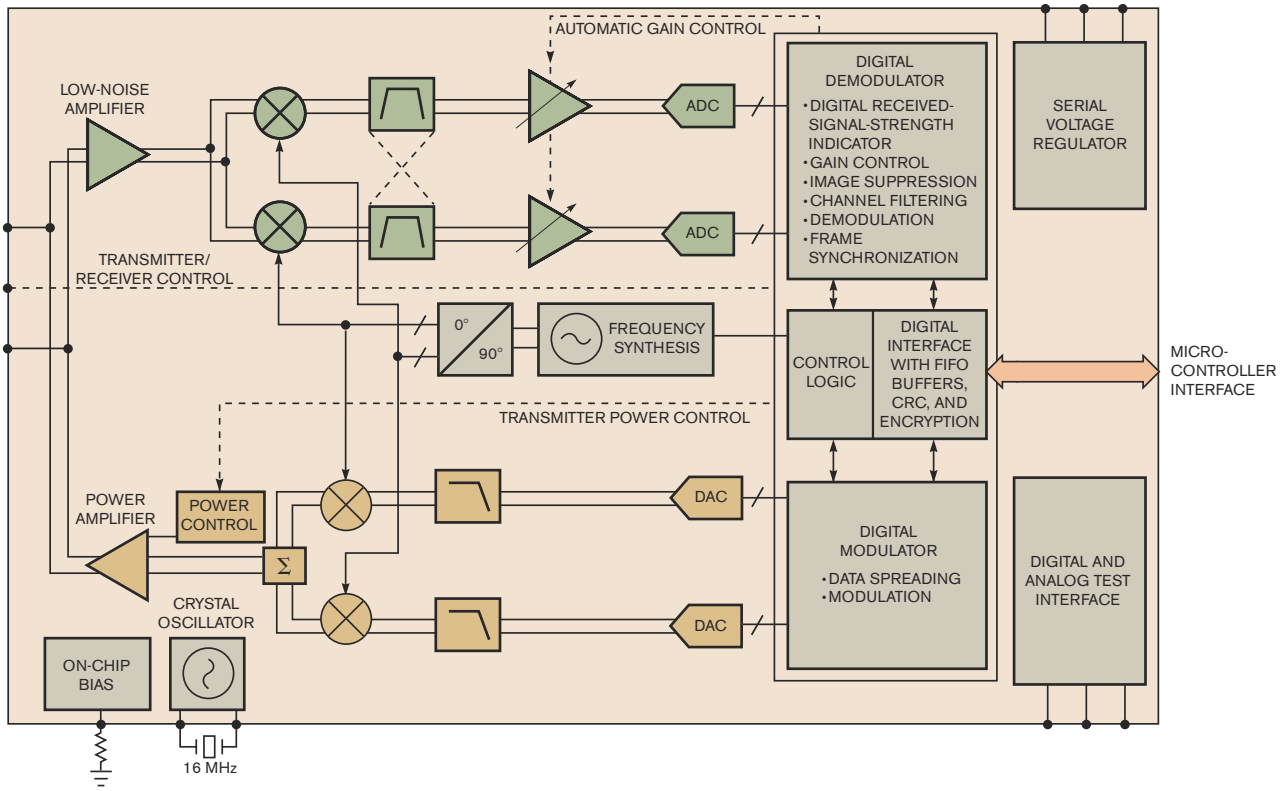

Figure 1 The 2.4-GHz, low-cost, low-power Chipcon CC2420 transceiver complies with both the IEEE 802.15.4 and the ZigBee standards.

Embedded Networking?
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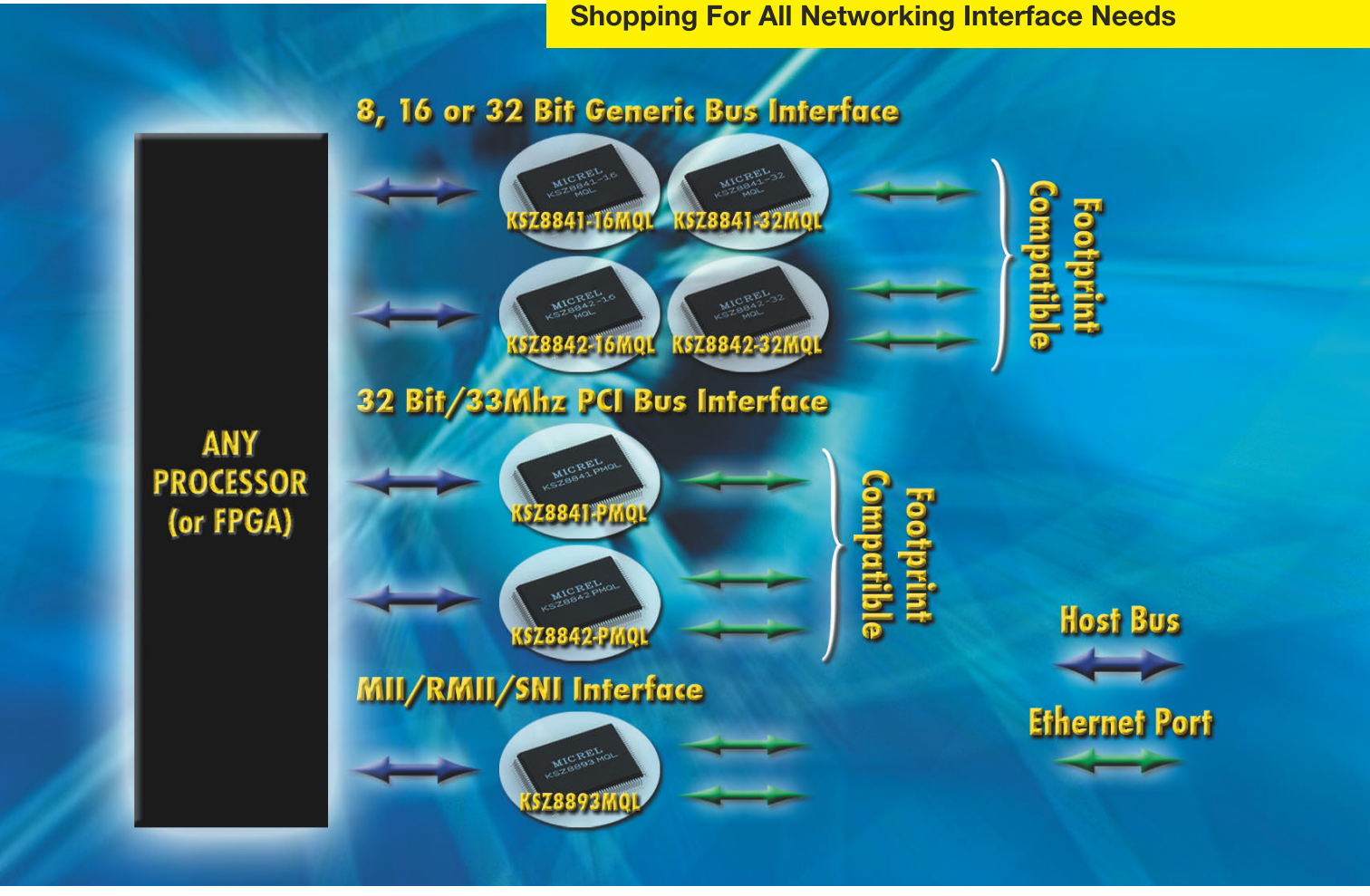
Micrel's KSZ88xx Series Gives Designers One-Stop Shopping For All Networking Interface Needs



The road to network connectivity is never smooth but Micrel has you covered. Whether you need networking via an 8, 16 or 32-bit generic-bus, PCI-bus, MII, RMII, or SNI host interfaces, Micrel has the answer in easy to install single and dual-port Ethernet solutions. The devices address the growing need for streamlined networking connectivity in IP-Set Top Boxes, VoIP phones, Network Printers, Industrial Controls and networked Game Console applications, to name but a few. The dual port devices have the lowest latency (sub 310nS) in the industry and are ideal for daisy-chaining applications, or simply as two port switches to connect to voice, video and data.

All of the ICs incorporate HP Auto-MDIX to take the guesswork out of whether your device is connected using straight or crossover cables. In addition, Micrel's LinkMD™ cable diagnostics function not only determines the length of the cable and the distance to fault, but also diagnoses common cabling faults such as open and short circuits. These features reduce the need for costly customer calls and IT service requests. Along with Micrel's trademark high reliability, outstanding performance, and low power consumption, the KSZ88xx family offers ideal solutions for applications that require compact, cost effective, RoHS compliant networking connections.

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the installation of new interconnecting cables. Another requirement of these isolated sensor nodes is extremely low power. In many remote locations, the sensors must run for as long as a year on battery power alone. These nodes can run on this reduced power because of the low data rates the sensors collect.

IEEE 802.15.4 defines an ultralow-power, low-data-rate wireless-network architecture that is ideal for many smart-building-sensor applications. Operating in the unlicensed frequency bands, the standard defines the PHY and MAC (media-access-control) sublayer specifications for low-rate devices communicating at 20 kbps in the 868-MHz band, 40 kbps in the 915-MHz band, and 250 kbps in the 2.4-GHz band. Networks may be arranged in star or peer-to-peer topologies and include addressing for more than 65,000 nodes. Transmitters use DSSS (direct-sequence spread spectrum) with BPSK (binary-phase-shift keying) in the less-than-1-GHz bands and O-QPSK (offset-quadrature-phase-shift keying) at 2.4 GHz. The standard provides for 16 channels in the 2.4-GHz band, 10 channels in the 915-MHz band, and one channel in the 868-MHz band. The specification describes two types of network nodes: an FFD (full-function device) that can perform any network duties and an RFD (reduced-function device) with limited resources and functions for cost-sensitive applications.

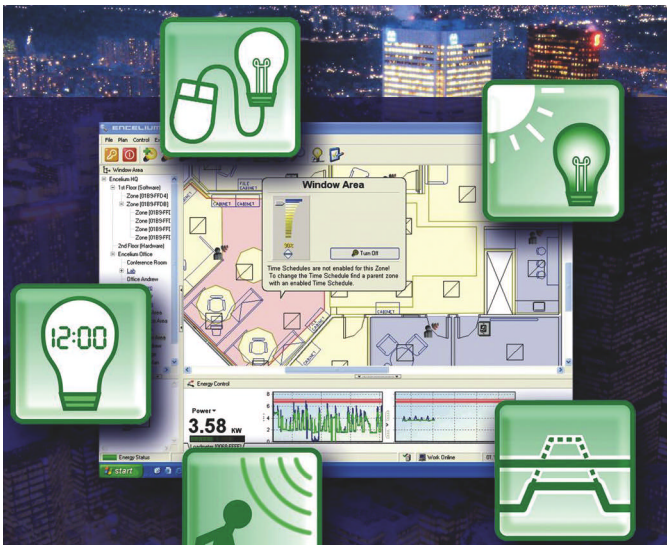

Figure 2 Encelium Technologies' Energy Control System promises to reduce commercial-building-lighting costs by as much as 70%.

LOW AND SLOW

Adding to the PHY and MAC layers that IEEE 802.15.4 defines, the ZigBee Alliance defined the remaining layers needed for low-rate, low-power wireless applications. Each network must have at least one FFD, or coordinator, to provide initialization, node management, and node-information storage. To minimize cost and power consumption, the remaining nodes can be the simple, battery-operated RFDs. You can use ZigBee networks with several data-transmission schemes. For periodic data, such as with wireless sensors, nodes wake up at set times, transmit sampled data to the coordinator, and go back to sleep. A light switch delivers intermittent data and may connect and communicate with the network only when you activate it. Repetitive-data applications, such as real-time-control systems, may use ZigBee's guaranteed-time-slot capability to ensure communications without latency or contention. These network-layer data-delivery strategies allow system designers to trade communications frequency for battery life in RFD nodes. Very low duty cycles allow nodes with coin-type batteries to remain operational for years.

ZigBee-compliant silicon and development tools are available from several semiconductor manufacturers. For example, the low-cost CC2420 transceiver from Chipcon targets low-power, low-voltage RF applications in the 2.4-GHz band (**Figure 1**). It complies with the IEEE 802.15.4 standard as well as the ZigBee requirements for interoperability. For secure applications, the CC2420 provides hardware support for data encryption and data authentication. Targeting low-cost host processors, the transceiver supports packet handling, data buffering, burst transmissions, address recognition, clear-channel assessment, and link-quality indication. The transceiver is suitable for FFDs and RFDs and includes a DSSS modem with a 250-kbps effective data rate. Current consumption is 17 to 18 mA with user-programmable output power. Reference designs with 0- and 10-dBm output power are available from Chipcon.

As building-automation products become more intelligent and interoperable, designers need a standard language to transfer requests, commands, and data between systems. Many designers settled on XML (Extensible Markup Language). Its text-based syntax is similar to highly successful HTML (HyperText Markup Language), which Web browsers use. Currently finding extensive use in Web-service delivery, XML encloses data within tags much like HTML, but with significant differences. Although HTML tags specify how to present or display text, XML tags describe the contents of the enclosed text. Another major difference is that XML is extensible, meaning that you can define your own tags.

Several manufacturers have incorporated XML into their lines of building-control products. For example, the federal government recently awarded Johnson Controls a contract to provide systems that control indoor environments at the new Library of Congress Motion Picture Broadcasting and Recorded Sound division building complex. The Johnson Controls XML-based Metasys building-management system will manage all temperature, humidity, and power loads. These Web-based environmental controls are critical for all audio and video recordings, especially films made on silver-nitrate film stock, which can deteriorate quickly and become potentially explosive at room temperature.

DEMAND RESPONSE

In a test of wide-area XML building-automation capabilities, researchers at the Department of Energy's Lawrence Berkeley National Laboratory (www.lbl.gov) completed an automated demand-response test to reduce electricity

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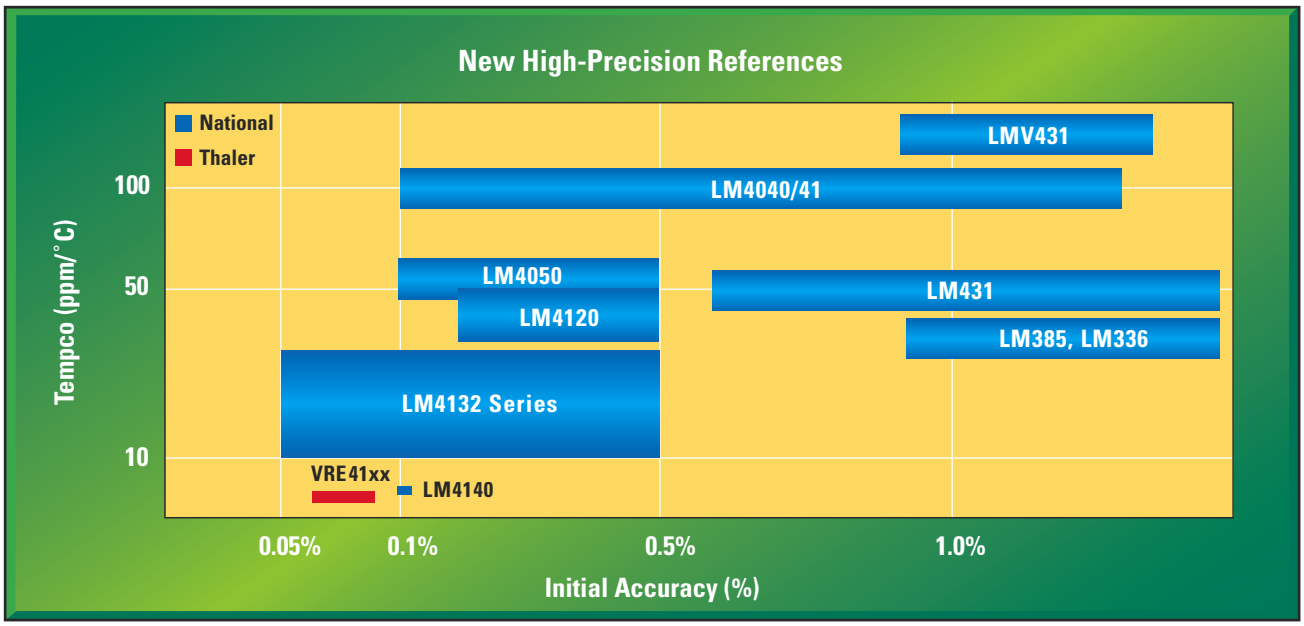

Product ID	Type	Initial Accuracy %	Tempco (max)	Quiescent Current	Noise
NEW **LM4132**	Series (LDO)	0.05% to 0.5%	10, 20, 30 ppm/°C	50 µA	125 μV_{PP}
LM4120	Series (LDO)	0.2%, 0.5%	50 ppm/°C	160 µA	24 μV_{PP}
LM4050	Shunt	0.1%, 0.2%, 0.5%	50 ppm/°C	39 µA	20 µVRMS
VRE41xx	Shunt (LDO)	0.05%, 0.08%	1 ppm/°C	230 µA	2.2 $\mu V_{P-P}/V_{OUT}$
LM4140	Shunt (LDO)	0.1%	3 ppm/°C	230 µA	4 $\mu V_{P-P}/V_{OUT}$

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consumption when high prices, blackouts, or excessive demand threaten the power grid. The test used XML signals over the Internet to indicate the current price per kilowatt-hour. As the price increased, a group of five large building facilities began to shed consumption by reducing lighting and air conditioning according to a prescribed plan. The successful test demonstrated that manufacturers' systems can listen to a common XML signal over the Internet and coordinate activities to reduce demand in case a power plant or transmission line fails.

In addition to XML, several other Internet technologies are important to building automation services, including the SOAP (Simple Object Access Protocol), the UDDI (Universal Description, Discovery, and Integration) format for application identification, and the WSDL (Web Services Definition Language). These technologies interact to form a software stack for locating, describing, and executing a Web service. You can view and download the latest standards for these Web-services protocols and technologies from the World Wide Web Consortium at www.w3.org.

The OASIS (Organization for the Advancement of Structured Information Standards) has proposed an initiative to define XML- and Web-services-based mechanisms for building-control systems. The OASIS oBIX (Open Building Information Exchange) technical committee is working to define a standard Web-services protocol to enable communications between building mechanical and electrical systems and enterprise applications. Because oBIX integrates with the enterprise, it allows continuous visibility of mechanical- and electrical-control systems and identifies problems and trends for system analysis or human interaction. The scope of the oBIX is to develop a Web-services-interface specification to simply and securely obtain data from HVAC, access control, utilities, and other building-automation systems. The oBIX approach has the advantage of operating with legacy mechanical and electrical subsystems.

Encelium Technologies' ECS (energy-control system) is an example of a scala-

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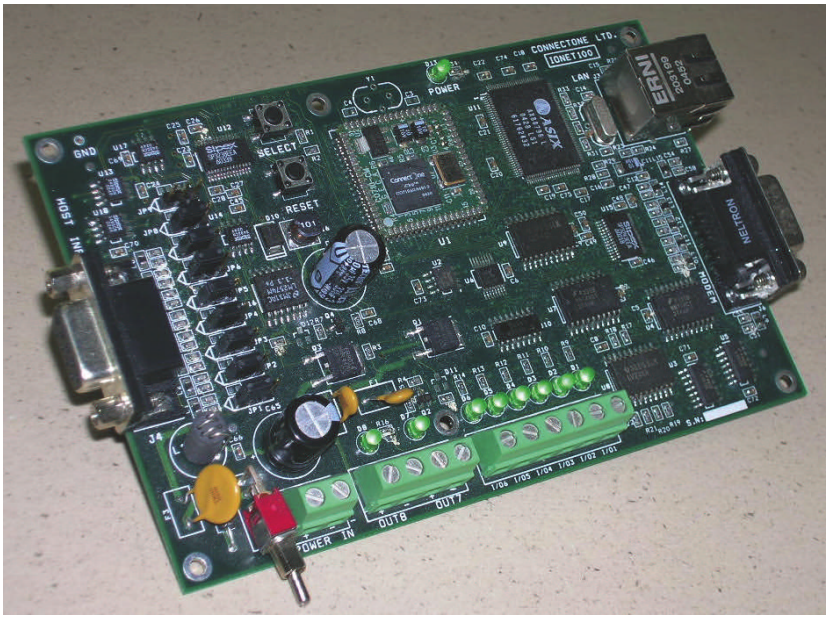

Figure 3 The ioNet embedded-device server module gives legacy industrial equipment or machines Web-based remote monitoring and control features.

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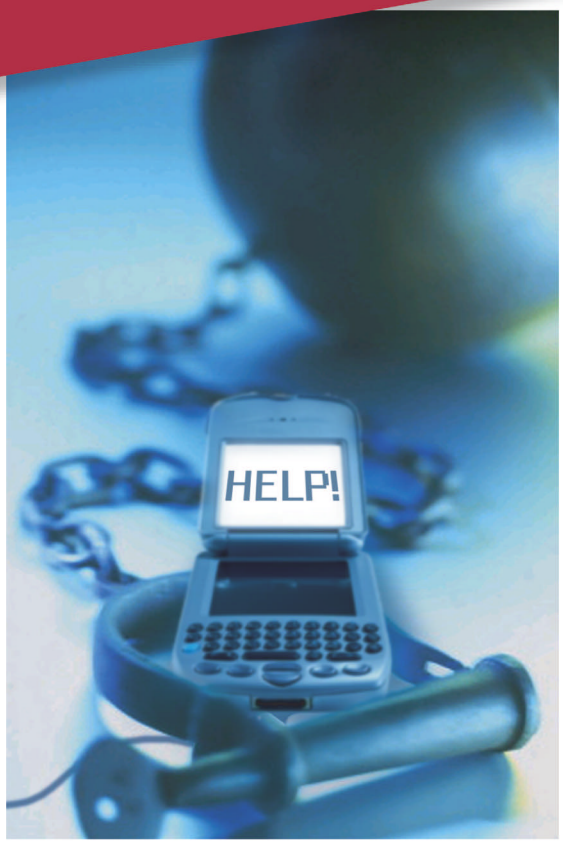


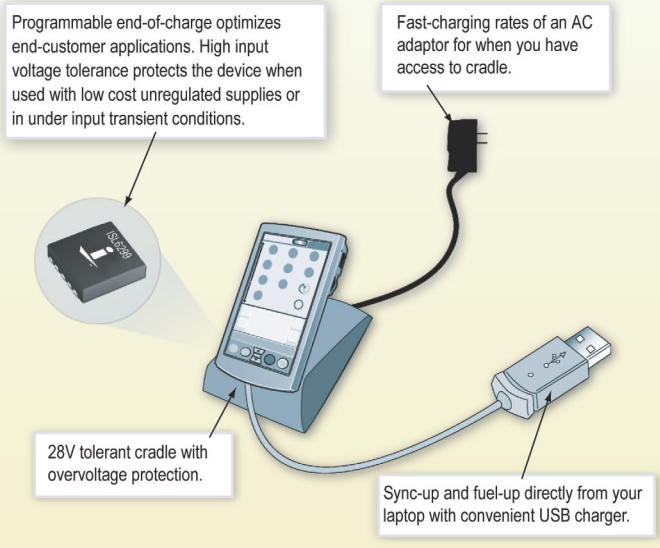
Intersil's ISL6299A is a fully integrated low-cost Li-ion or Li-polymer battery charger that accepts both USB port and desktop cradle charger.

The ISL6299A is a low component count solution that features programmable cradle charge current, charge indication, adapter present indication, and programmable end-of-charge (EOC) current with latch. All these advanced features, along with Intersil's Thermaguard™ technology for an added measure of thermal protection, are delivered in a single 3x3 mm DFN package.

ISL6299A System

Cradle input. The max input voltage tolerance is 28V. Programmable charge current up to 1A and programmable end of charge current. The included end of charge latch is the default input source.

USB input. Takes input from USB port or other low voltage supply. Fixed charge current at typically 380mA. Only charges when cradle source is not connected.



ISL6299A Key Features:

- Dual-input charger for single-cell li-ion/ polymer batteries for cradle and USB
- Low component count
- Integrated pass element
- Fixed 380mA USB charge current
- Programmable cradle charge current
- Charge current Thermaguard™ for thermal protection
- 28V maximum voltage for the cradle input
- Charge and adapter presence indicators
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ble hardware and software system that allows users to reduce lighting requirements with photosensor-based automatic-lighting-level adjustments, occupancy sensor-based lighting levels, time-based zone-lighting control, and load shedding through dimming to accommodate energy-price spikes. The system's communication network allows employees or building-energy managers to individually control light fixtures, occupancy sensors, photosensors, and wall dimmers from a PC or through the Internet. The graphical user interface for the ECS comprises Encelium's central-control software, which allows any workstation to perform direct lighting control and other energy-management functions through the facility's LAN wiring (**Figure 2**). The price of the ECS starts at $10,000, depending on system configuration.

In today's building-automation climate, designers must deal with numerous stand-alone subsystems that lack any communications capability. Connect One offers the ioNet embedded-device server module, which uses Internet protocols to retrofit installed industrial equipment or machines with remote-monitoring and -control features (**Figure 3**). The module allows system designers to interface devices—such as elevators, surveillance cameras, vending machines, and gaming machines—that lack built-in communications hardware. Users can hard-wire the output from digital or analog signals in the device to ioNet's terminal block. The module can then log events and exchange data over the Internet through a built-in 10/100BaseT port. You can remotely manage ioNet over the Web by a standard browser or by Connect One's device-connectivity server.

Because of the longevity of real estate, smart-building technology will take years and even generations to become a dominant part of our architectural inventory. During this transition period, designers must devise clever techniques to deliver the benefits of building automation without complete replacement of legacy systems. Today, Web technology seems to be the favored approach to allowing incompatible systems to share data, respond to remote commands, and be a part of the business-information architecture. EDN

You can reach Technical Editor Warren Webb at 1-858-513-3713 and wwebb@edn.com.

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- V_{OUT2}: **Adjustable, 0.8V to V_{IN}**
- V_{OUT3}: **Adjustable, 0.8V to V_{IN}**

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Triple Output PWM Controller
4.5V to 5.5V or
5.6V to 24V
Input Voltage

- V_{OUT1}: **Adjustable, 0.8V to V_{IN}**
- V_{OUT2}: **Adjustable, 0.8V to V_{IN}**
- V_{OUT3}: **Adjustable, 0.8V to V_{IN}**

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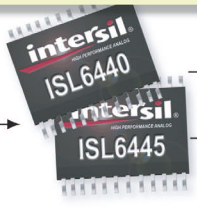

- V_{OUT2}: **Adjustable, 0.8V to V_{IN}**
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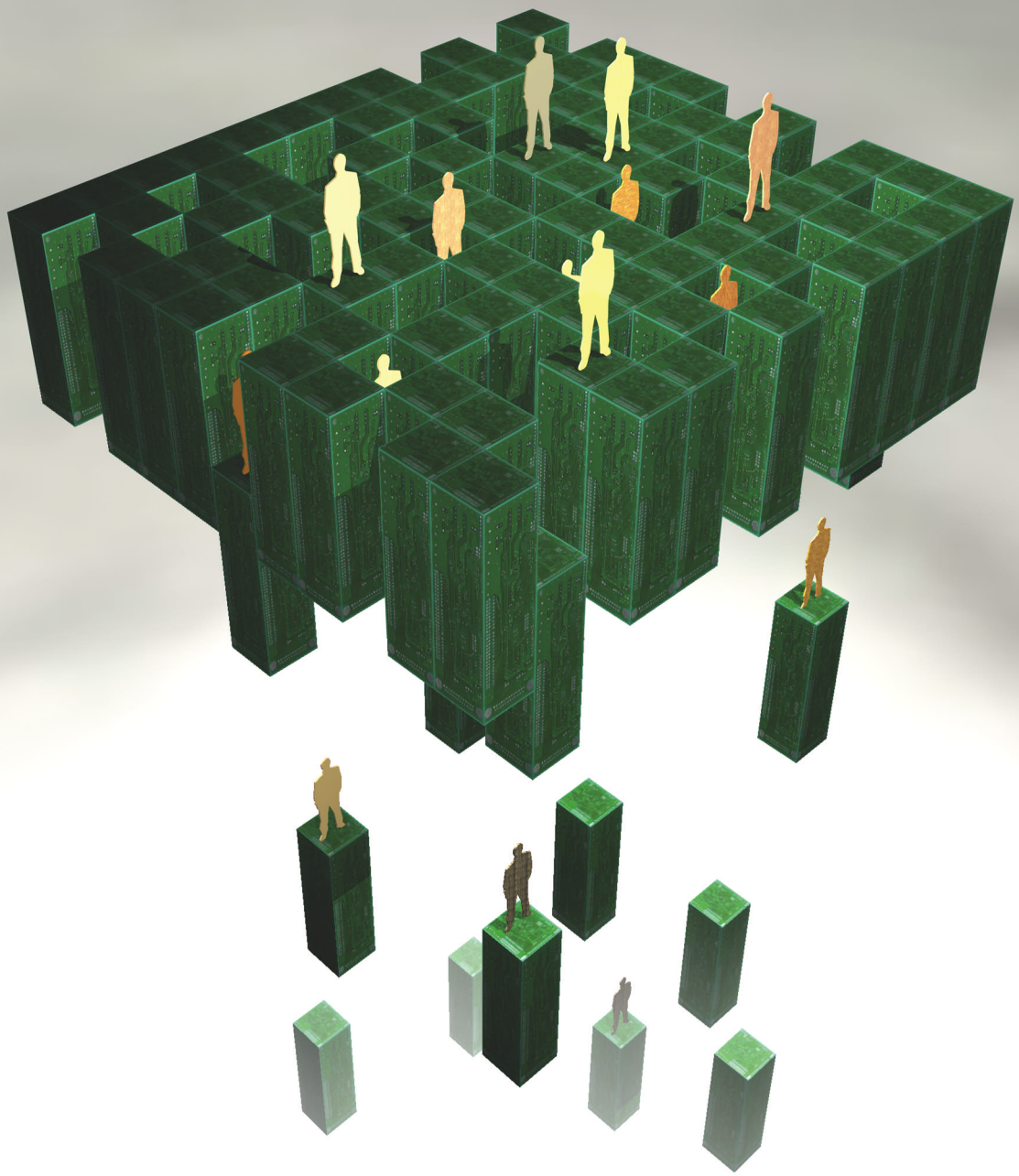


BY MICHAEL SANTARINI • SENIOR EDITOR

WITH NEW DFM-TOOL COMPANIES POPPING UP EVERY MONTH, IT CAN BE HARD TO SELECT WHICH YOU NEED FOR 65-NM PROCESSES. BUT THE TOP THREE FOUNDRIES AT THAT NODE HAVE MADE SOME OF THE CHOICES FOR YOU.

SIFTING THE DFM PLAYERS

Does DFM stand for "design for manufacturing" or "design for marketing"? That's a question many observers of the EDA industry have been asking ever since someone uttered the term a few years ago. At the 130-nm node, lithography equipment could no longer clearly print certain semiconductor features, and OPC (optical-proximity-correction) tools from EDA vendors such as Numerical Technologies and OPC Technologies came to the rescue. As design processes have continued to shrink to 90 and 65 nm, lithography, mask-making, and fabs have become even more reliant on EDA-vendor inventions and fixes in design tools to ensure the accurate manufacture of chips. Fabs are turning to EDA tools even to help improve yield, which was once the sole responsibility—and a big selling point—of the fabs.

AT A GLANCE

- Fabs now provide varying degrees of process and lithography data to DFM (design-for-manufacturing)-tool vendors.
- TSMC (Taiwan Semiconductor Manufacturing Co), UMC (United Microelectronics Corp), Chartered, IBM, and Samsung posted $13.5 billion in fab revenue in 2005, according to Gartner.
- The entire fab segment posted revenue of $18.4 billion, according to Gartner.
- If you buy the fab-recommended DFM tools, you will need at least $1 million more than what you would pay for traditional tools.
- Rules-based lithography simulation and analysis are giving way to model-based approaches as designs move to the 65-nm node.

As such, the EDA industry, which has remained in a $4 billion-in-revenue rut for the last four years, has identified DFM as a promising avenue of growth. That assertion recently received its strongest confirmation as the three biggest foundries employing 65-nm processes—TSMC (Taiwan Semiconductor Manufacturing Co), UMC (United Microelectronics Corp), and the CIS (Chartered/IBM/Samsung) Alliance—have all added a number of DFM technologies to their reference flows. In doing so, they are putting some of the burden to improve fabrication quality and yield on designers.

Luckily, plenty of EDA vendors are willing to provide you with DFM tools. Indeed, it seems that at least one new DFM start-up emerges every month, announcing itself to the world with claims of having essential technology. Meanwhile, some established companies have miraculously re-emerged as DFM vendors with few changes to legacy technologies but many changes to their marketing literature. And the big EDA vendors—Cadence, Synopsys, Mentor, and Magma—have aggressively added DFM technologies and features to their established flows and have even reclassified as DFM some tools—mostly from the physical-design, physical-verification, design-for-test and TCAD (technology-computer-aided-design) lineups.

By June, research company Gartner Dataquest (www.gartner.com) had identified 16 DFM companies offering tools that layout engineers would use. Those companies are Anchor Semiconductor, Aprio Technologies, Blaze DFM, Brion Technologies, Cadence, ChipMD, Clear Shape Technologies, Ponte Solutions, Magma Design Automation, Mentor Graphics, Nanno Solutions, Nannor Technologies, Predictions Software, Sigma-C, Synopsys, and Xyalis. The list does not include vendors of statistical-timing tools, but it should (see **sidebar** "Statistical timing will become DFM"). The DFM segment of the EDA market has become so large that several subcategories of DFM now exist.

With all this in mind, you may be wondering what tools you will need to purchase to implement a design at 65 nm. If you want to do it right, the short answer is that you are going to need several tools. Oh, and bring your checkbook, too; it's going to be expensive.

Most of the dozens of IDMs (integrated-device manufacturers) don't publicly reveal what DFM companies they are working with or what technologies they have built on their own. But one way to separate the wheat from the chaff in DFM is to examine which tools the foundries say you will need to get the best performance from 65-nm silicon. By press time, three of the top four foundries—first-ranked TSMC, second-ranked UMC, and fourth-ranked CIS Alliance—will have released their 65-nm reference flows. SMIC, the third-largest foundry, is now getting its 90-nm process up and running, but you can bet that it will soon be working on a 65-nm technology.

TSMC, UMC, Chartered, IBM, and Samsung posted a combined total of $13.5 billion in fab revenue in 2005. The entire fab segment posted revenue of $18.4 billion, according to Gartner. If that trend continues, the five fabs will likely manufacture the bulk of 65-nm ICs. None of the foundries says that it is necessary that you buy DFM tools to implement 65-nm silicon. You could use your 90-nm tool flow, they claim, but all strongly suggest that you buy "recommended" DFM tools if you want to quickly get the most out of their 65-nm processes.

PROCESS DATA IS CRUCIAL

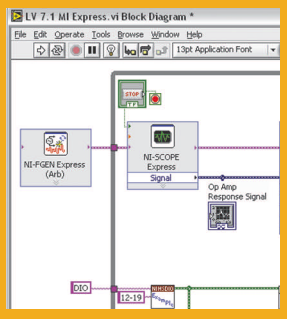
A couple of years ago, foundries were less than willing to share their sensitive defect density, yield data, and lithography models with EDA vendors, especially start-ups, fearing that the data would end up in competitors' hands. To their credit, TSMC, UMC, and the CIS Alliance foundries have been more than willing to give EDA vendors this data, with varying degrees of disclosure and protection.

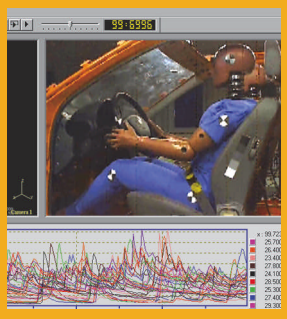
According to Ed Wan, senior director of design-services marketing for TSMC,

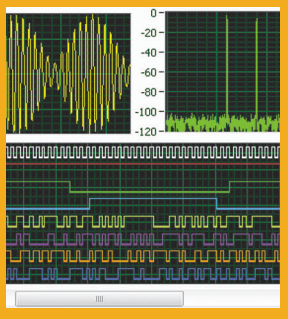
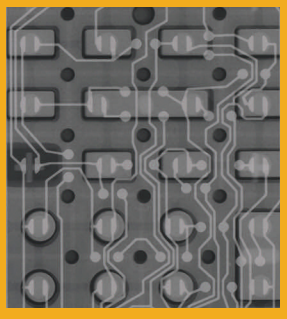
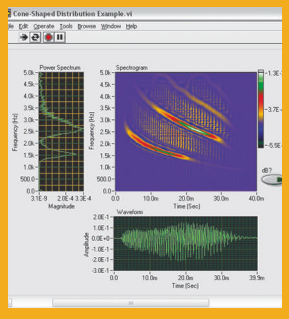
STATISTICAL TIMING WILL BECOME DFM

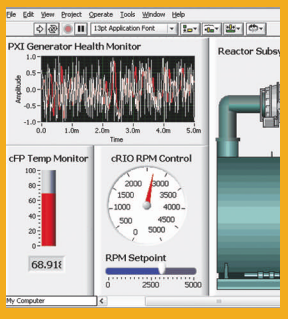
SSTA (statistical static-timing analysis) is promising technology, but its role and importance in the tool flow will likely evolve as the technology matures. It's likely that users will employ early SSTA tools to get a better idea of the true timing of circuits, rather than rely on worst-case timing models, which fabs provide in the form of wire-load models. The first evolution of SSTA will supplement static-timing tools and perhaps even replace them as sign-off tools.

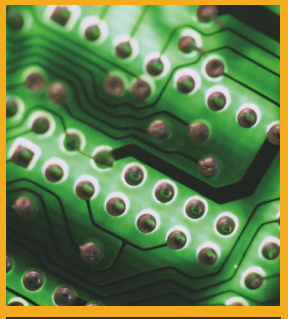
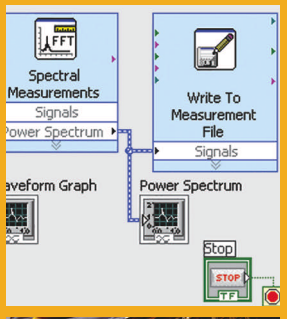
SSTA-tool developers hope that the tools will one day enable engineers to make trade-offs among timing, power, and yield early in the design cycle. For example, squeezing high performance from a design may involve penalties to the design's power targets and reduce yield. But if they skimp on timing, they may see better yield and lower power consumption. Companies offering commercial SSTA include Altos Design Automation, Extreme DA, IBM, Magma, and Synopsys.

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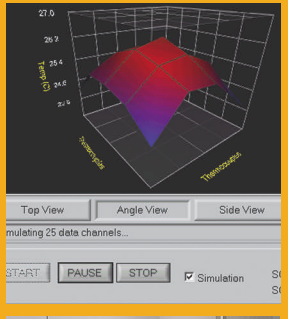



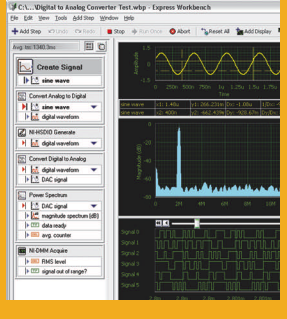

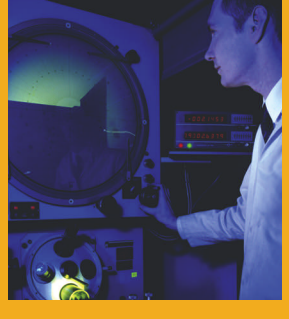
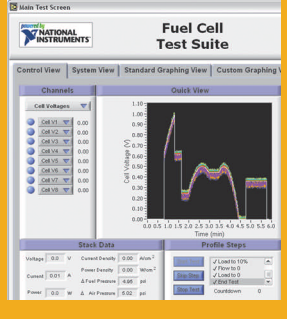

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two years ago, TSMC recognized that sharing data with EDA vendors would be essential to the success of 65-nm silicon and EDA-DFM-tool development. TSMC this year unveiled its DDK (DFM Data Kit) and DUF (DFM Unified Format), which encapsulate data for LPC (lithography-process check), CMP (chemical-mechanical-polishing) analysis, and CAA (critical-area analysis). Devising this common format allows TSMC to work more closely with established EDA vendors but also provide up-and-coming tool vendors in the EDA market with solid data to try to make their tools comply with TSMC's 65-nm flow.

UMC has no common data format per se, but it does provide yield data to EDA vendors and selected customers. "We don't use absolute yield; we provide relative-yield information," says Patrick Lin, chief SOC (system-on-chip) architect for system and architecture support at UMC. "We don't provide direct data; rather, it's encrypted. Some tool companies don't require a lithography model, but, if they do, we encrypt it. We don't think format is an important issue, as others do," he says. "Our goal is to just get a few tools ready for customers. To provide a solution to our customers is important; to provide a data format is not. If the whole industry is targeting a standard format, we're willing to participate."

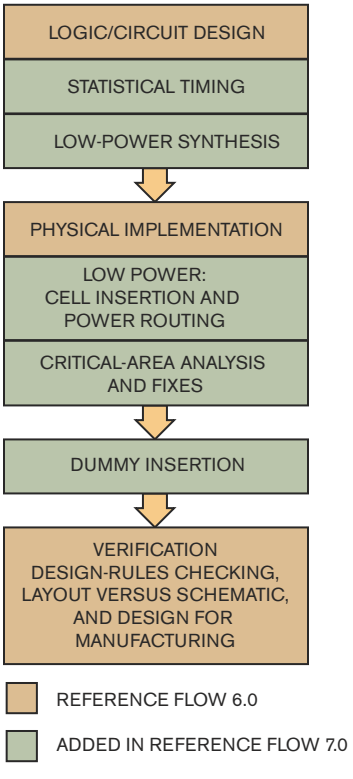

Figure 1 TSMC's 7.0 reference flow adds SSTA, DFM, and power management.

ALL THREE FOUNDRIES HAVE EVALUATED THE COMMERCIAL DFM OFFERINGS IN AN ATTEMPT TO SHAPE THEIR DFM FLOWS FOR CUSTOMERS.

The founders of the CIS Alliance formed the group to ensure that all three companies' 65-nm fabs were similar and thus worked from the same process rules and data format. The alliance has made available model kits that contain sensitive fab data in encrypted formats. Fab data in these model-based kits are for CAA, shape simulation, and CMP simulation.

RECOMMENDED TOOLS

In creating their 65-nm flows, TSMC, UMC, and the CIS Alliance all have been working closely with the big four in EDA—Cadence, Synopsys, Mentor, and Magma—to ensure not just that the four have the DFM-point tools, but also that their flows synchronize with the new processes. The three foundries, however, differ in which point-tool companies they work with. In general, UMC works with any point-tool vendor that its customers want. TSMC, as in years past, has developed a reference flow for 65 nm outlining how Cadence's, Synopsys', or Magma's flows work with TSMC. The TSMC reference flows also include tools from smaller companies in case those three EDA vendors' flows don't provide the functions that TSMC recommends. This year, TSMC also created a DFM-compliance program in which it provides its DDK files to start-ups so that they can develop future DFM technologies. Somewhat as a result of its common-foundry format, the CIS Alliance has extensively evaluated available commercial-EDA tools and strongly recommends that its customers use its suggested list of vendors. With 16 independent EDA vendors to choose from, all three foundries have evaluated the commercial DFM offerings in an attempt to shape their DFM flows for customers.

TSMC REFERENCE FLOW

Every year, TSMC issues a new reference flow, which helps users get a better idea of design challenges and which tools they need to design for a given node. At last month's Design Automation Conference in San Francisco, TSMC unveiled reference flow 7.0, enabling customers to use flows from Cadence, Synopsys, and, new this year, Magma to design 65-nm ICs targeting TSMC's foundry (**Figure 1**). As in years past, the reference flow includes DFM and low-power tools. This year, however, TSMC also recommends that users buy SSTA (statistical-static-timing-analysis) tools, arguably a subcategory of DFM.

For years, TSMC has been driving the big vendors to ensure that their tools support its 65-nm process, according to Wan. Cadence, Synopsys, and Magma now all have complete DFM flows, so, if users want to go with single-vendor, all-in-one flows, TSMC verifies that their flows comply with TSMC's 65-nm process, he says. Synopsys and Magma already comply with TSMC's stipulation for SSTA. Cadence, on the other hand, is not yet fielding an SSTA technology. Cadence also until recently lacked a CMP-simulation technology but recently acquired CMP-simulation tool Praesagus to tie up that loose end.

In addition to its reference flow, TSMC has also announced a DFM-qualification program to ensure that third-party-DFM vendors also offer compliant tools. For lithography-process characterization and simulation, TSMC has thus far qualified Anchor Semiconductor's NanoScope DFP, Cadence's Virtuoso RV, Clear Shape's InShape, Magma's Blast Yield TX, Mentor Graphics' Calibre LFD (lithography-friendly design), and Synopsys' DFM LCC (lithography-compliance checking). For CMP simulation, TSMC has qualified Cadence/Praesagus Solutions'

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DVIP, Magma's Blast Yield TX, and Synopsys' DFM-CMP. For CAA, TSMC has qualified Cadence's Encounter-CAA, Magma's Blast Yield TX, Mentor's Calibre YieldAnalyzer, Ponte's Yield Analyzer, Predictions Software's Eyes, and Synopsys' IC Compiler. TSMC will add other companies over the coming months.

Wan says that TSMC is well-aware that many users want to use a mixed-tool flow or may be developing their own. For this group, TSMC provides a reference kit that combines scripts, application notes, and test cases. Meanwhile, TSMC recommends Blaze DFM for simultaneous power and yield enhancement.

UMC's FLOW IS FLEXIBLE

UMC says that some DFM-tool functions are necessary for its 65-nm flow, especially those technologies adding functions to placement and routing, but other DFM tools are not yet necessary for sign-off. "Within DFM, there are a lot of different levels, and the needs of customers vary," says Lin. "Some require DFM tools, but they are not using them for sign-off but as learning tools for future processes. Customers can take advantage of some tools to improve their 65-nm designs." UMC will work with any EDA vendor customers ask for, but the company does have a reference flow (**Figure 2**). "In our reference flow, we recommend the functions they should look at, but, as far as EDA vendors go, it's the customer's choice," says Lin. "Some of these tools need to tie closely to foundries. The tools must be accurate, and we've worked closely with some vendors to achieve that goal."

"ANYTHING TO DO WITH ROUTING IS ESSENTIAL, AND, ONCE YOU ARE TALKING ABOUT ROUTING, THEY NEED TO KNOW LITHOGRAPHY, CAA, AND NORMAL DFM RULES."

DFM functions for routers, such as metal fill, double-via insertion, and wire spreading, are essential, says Lin. In this area, the company has been working closely with Cadence, Synopsys, and Magma. "Anything to do with routing is essential, and, once you are talking about routing, they need to know lithography, CAA, and normal DFM rules," says Lin. CAA is also growing in importance, he says. "It is an area in which the fab needs to provide relative-yield data," he says. "These tools allow customers to make a trade-off from a cost point of view. Customers often pressure us to provide some data." Two types of DFM technologies to help enhance lithography are also growing in importance, he notes. The first includes tools that can identify potential lithography hot spots in the physical-design steps. The second includes tools that identify lithography's impact on shape. "We need these tools so that we can calculate what impact a given shape change will have on electrical properties," says Lin. "That will take some time. Designers would love to have those tools, but a unified system doesn't yet exist." He says that UMC is working on that problem with Mentor Graphics, Clear Shape, and Anchor Semiconductor.

CMP simulation is also gaining importance. "CMP is a tricky area," says Lin. "For large designs, we will see some flatness issues, and that's where CMP simulation is necessary. In the early stage of the process, the flatness won't be good, but, as the process matures, it will be." He notes that it is helpful to have a CMP model for extraction tools so that they safely reflect the interlayer capacitance and series resistance of the interconnect. The company has been working most closely in this area with Cadence's recent acquisition, Praesagus, but Synopsys and Magma claim to also offer this technology.

SSTA is another promising area, says Lin. "I don't believe people will use it to sign off the design as yet," he says. "They will use the SSTA to tighten the on-chip-variation global margin. That's a first step. Maybe in the future nodes, they will make it a standard sign-off tool." The company has been working closely with SSTA start-up Extreme DA. The company is also working with Apache Design on thermal analysis, which can impact power and yield. Lin also notes that IP (intellectual property) and IP tools must also become more lithography-friendly and more adaptable to manufacturing.

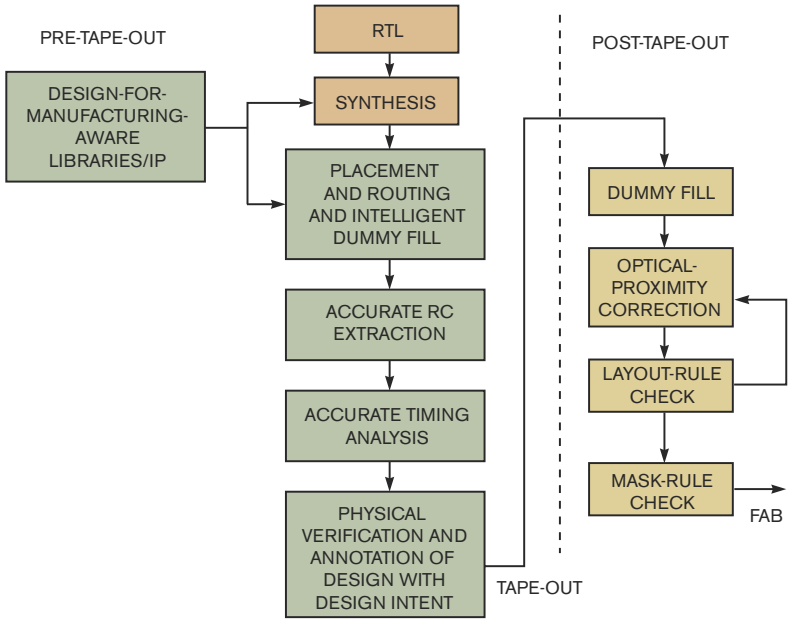
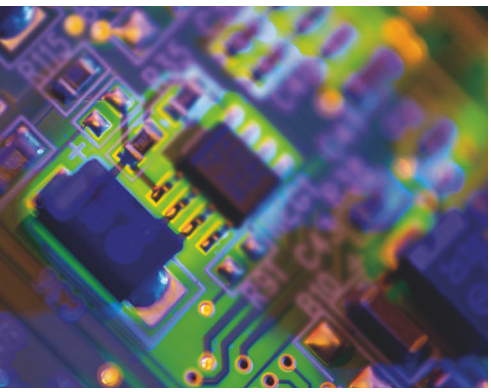
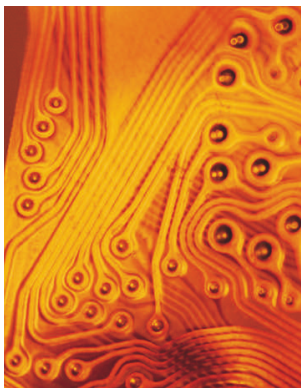


Figure 2 UMC's DFM flow stresses DFM-aware IP in addition to new tools.

CIS SPECIFIES DFM TOOLS

While TSMC and UMC have been establishing flows and are open to working with newcomers, the CIS Alliance has been doing a lot of the evaluation work for customers. Doing so seemingly





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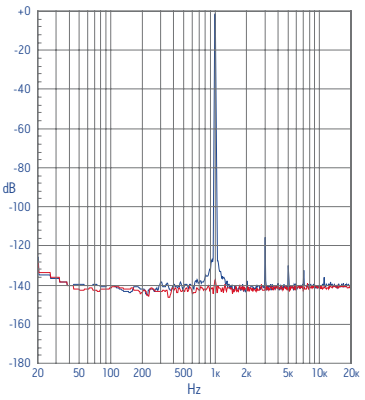

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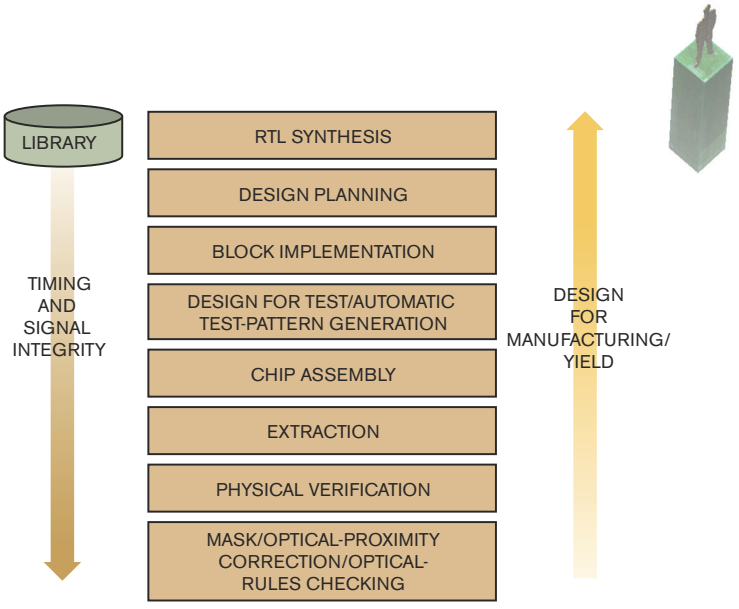

Figure 3 The CIS Alliance selected a DFM flow.

saves customers time in evaluating tools, but it also ensures that customers can ship their designs to Chartered, IBM, or Samsung fabs—likely with necessary adjustments to GDSII (Graphic Design System II) files and masks. Walter Ng, senior director for platform alliances at Chartered Semiconductor Manufacturing, says that when the CIS Alliance emerged last year, the three companies created eight subcommittees focusing on DFM-design guidelines: CAA, reference flows, lithography-based simulation, shape-based simulation, variation-aware timing, DFM services, CMP simulation, and DFM checking. Each subcommittee evaluated third-party tools and ran through evaluations to come up with a flow (**Figure 3**). "We selected the best technologies out there at least at the time the evaluations were done," says Ng.

In the DFM-checking area, Chartered selected Mentor Graphics in the back-end for OPC, RET (resolution-enhancement technology), and lithography. "Even though it is a rule-checking tool, we still see it as a critical piece," says Ng. "We don't believe we can move completely from rules to model-based approaches." The company selected Mentor Graphics Calibre DFM, which is now the YieldAnalyzer tool. "We've weighted the recommended rules, so folks can run their layouts through the checking deck," says Ng. "It allows them to bin the highest priority rules and then focus on where they are going to fix the layout for those highest return-on-investment areas and then rerun it and see that the relative scoring has improved for that cell or block."

For CAA, Chartered selected Ponte Solutions' model-based approach that accounts for defect densities on a per-layer basis. "The Ponte tool was at the time the most accurate in CAA and identifying hot spots," says Ng. In the reference-flow area, the company is working with Cadence, Synopsys, and Magma. "They are all looking at ways to make their routers more intelligent and do a correct-by-construction approach," says Ng. CMP simulation and fill capability offer accurate parasitic extraction, providing feedback to timing analysis and signal integrity to ensure that fill is uniform. The alliance picked Cadence's Praesagus tool for this purpose.

The CIS Alliance uses Mentor Graphics' LFD for shape and lithography simulation. The collaborative project helps designers locate potential trade-offs and effects on manufacturability, Ng notes. "We have been working with them to make sure that a product does what we expect from it," says Ng. "The product is highly accurate because the input to it is the actual OPC deck." The CIS Alliance is also working with Clear Shape in shape and lithography simulation. Because it works with an abstracted model, Clear Shape has greater capacity and performance than Calibre LFD, but the alliance deems the Mentor tool to be more accurate, says Ng. "Calibre LFD can be accurate, and Mentor is always enhancing its capabilities in accuracy, performance, and capacity," he says.

No tools exist for DFM-layout guide-

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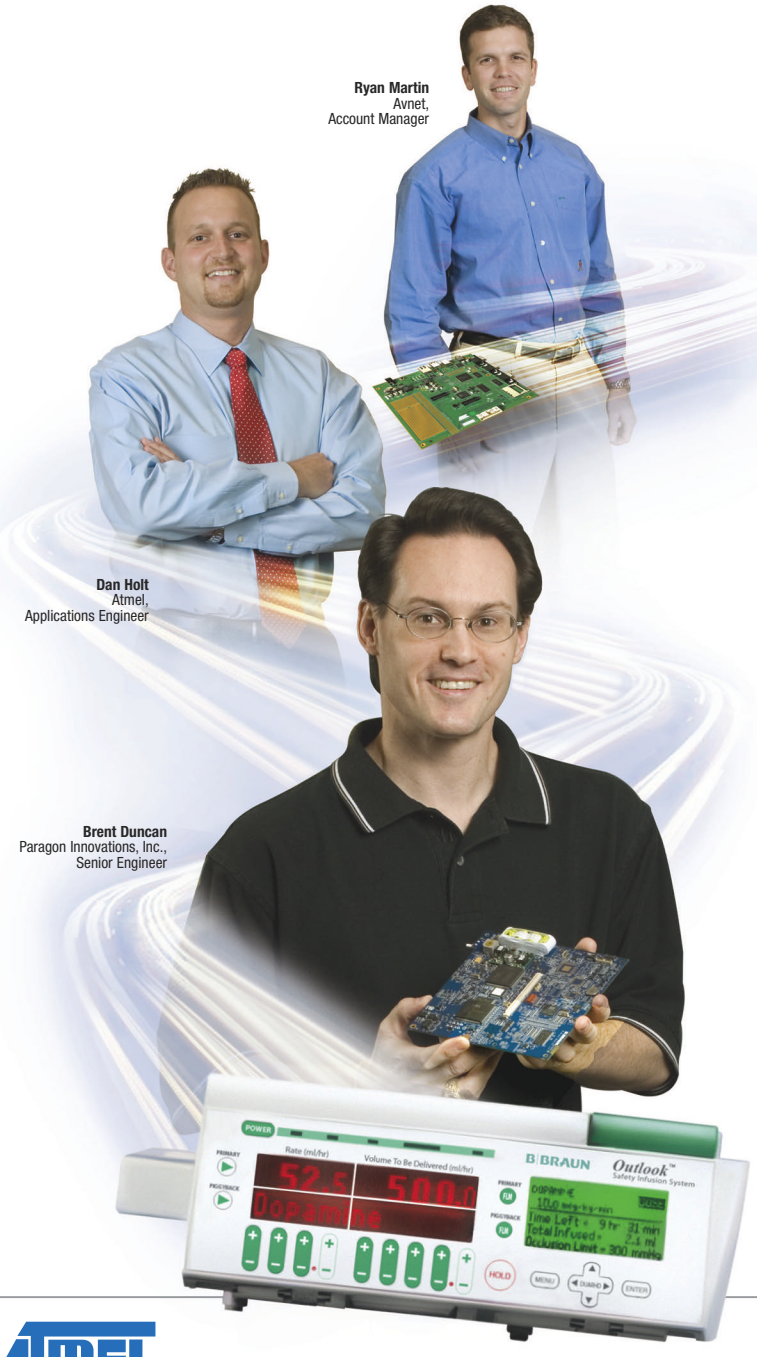

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lines, but the CIS Alliance believes it has an advantage over competitors in this area by virtue of its common platform. "We have dedicated chapters to layout recommendations for manufacturability," says Ng, who points out that the alliance augments these recommendations as more designs, targeting different applications, go through fabs. "Between Chartered, IBM, and Samsung, we get to see a range of designs at various complexities," says Ng. "We've collaborated to bring together a DFM-layout-guideline document for our clients, and we update that a couple of times a quarter to make sure that the document encapsulates the latest observations and learning."

The CIS Alliance has also been working closely since last year's DAC with Blaze DFM for leakage reduction and yield optimization. "We have been working with some of our major customers with Blaze to demonstrate proof and value, and we've gone through some silicon, and that is promising technology," says Ng.

The CIS Alliance does not name the company it is working with for SSTA. However, it will likely get this technology from IBM, which has for years performed acclaimed research in SSTA. IBM's SSTA-tool-development group won the 2005 *EDN* Innovator of the Year award, and the group last year introduced an SSTA tool, but the technology has yet to appear in commercial flows outside IBM. "We are doing some work in that area, and we didn't announce a technology because we haven't yet produced a deliverable for the common process yet," says Ng. Although some of the technologies may become mandatory, right now it's a trade-off. "The designers know better what they are willing to trade off against what," says Ng. "In this case, yield is one of the trade-off vectors at stake. Customers say, 'All I expect you guys to do is see what those trade-offs are, and I'll make those trade-offs and enable the data to make these tools work.' At some point, these tools may become critical. I can, for example, see that some of these technologies may end up augmenting DRC (design-rule checking). It is becoming more difficult, and the design rules for 45 nm are restrictive." He says that encapsulating the rules files requires large DRC decks.

NOW, THE BAD NEWS: COST

If you add up the reported minimum cost of these tool flows, you come up with a sum of $1 million to $3 million for just one license of each point tool. For example, Blaze DFM's tool costs $2 million for a one-year site license. Prices for the other DFM tools range from $100,000 to $250,000 for a single annual license. However, at every node, overblown hype regarding the cost of tools emerges, according to the foundries. Ng points out, for example, that hype sur-

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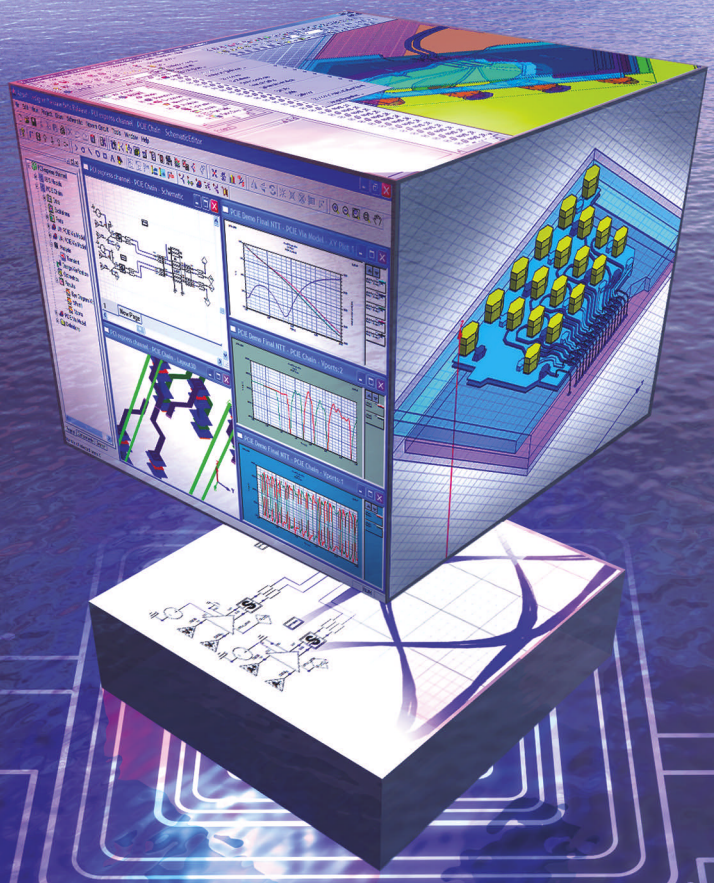

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rounded the emergence of signal integrity and the resultant retooling it required but that vendors eventually integrated the technology into the larger EDA-tool sets. "Some of these capabilities will go the same way, and vendors will build them into existing tools," says Ng. "There is certainly more consolidation to happen. Some of these DFM companies may find it hard to hang around as independent companies without being tightly coupled to these larger integrated solutions."

UMC's Lin points out that some of these functions are becoming more important and, in some cases, require users to purchase them in addition to the traditional 90-nm flow. He notes, however, that existing tools will absorb some of these features and that the company will solve some of these problems in the fab. "We didn't push that much of the burden to designers," he says. "But there is some benefit to push some of it to designers. We're trying to work from the fab side to reduce problems and pass information to them, so that they can better use the flow. They don't have to be scared. I want to stress that it's the traditional flow; it's an add-on. There isn't much more the designer needs to do." With CMP, for example, designers need only a technology file from the fab to run SSTA.

Now that DFM has established itself, as with other EDA technologies, such as power and timing, EDA vendors will come up with technologies to allow designers to address manufacturing earlier in the flow—at floorplanning, for example, or even in the RTL (register-transfer level). Driving the correct-by-construction approach and making sure IP cores and foundation elements are DFM-ready will become necessary.

DFM is addressing problems and, therefore, at least for the 65- and 45-nm nodes, is becoming an avenue of growth for the EDA industry. Most vendors agree that nice-to-have features today in DFM for the 65-nm node will likely become must-have features as the industry moves into the 45-nm node and below. It will be interesting to see whether standard tool flows absorb most of the DFM EDA technologies and whether the EDA vendors can successfully ensure that their tools account for most of the nasty DFM issues. It will also be interesting to see whether foundries can get the upper hand on many of these manufacturing issues, so that when you refer to DFM, you see it as a way to home in on performance, power, and yield targets rather than as an extra task you need to perform to make up for the shortcomings of the foundries. EDN

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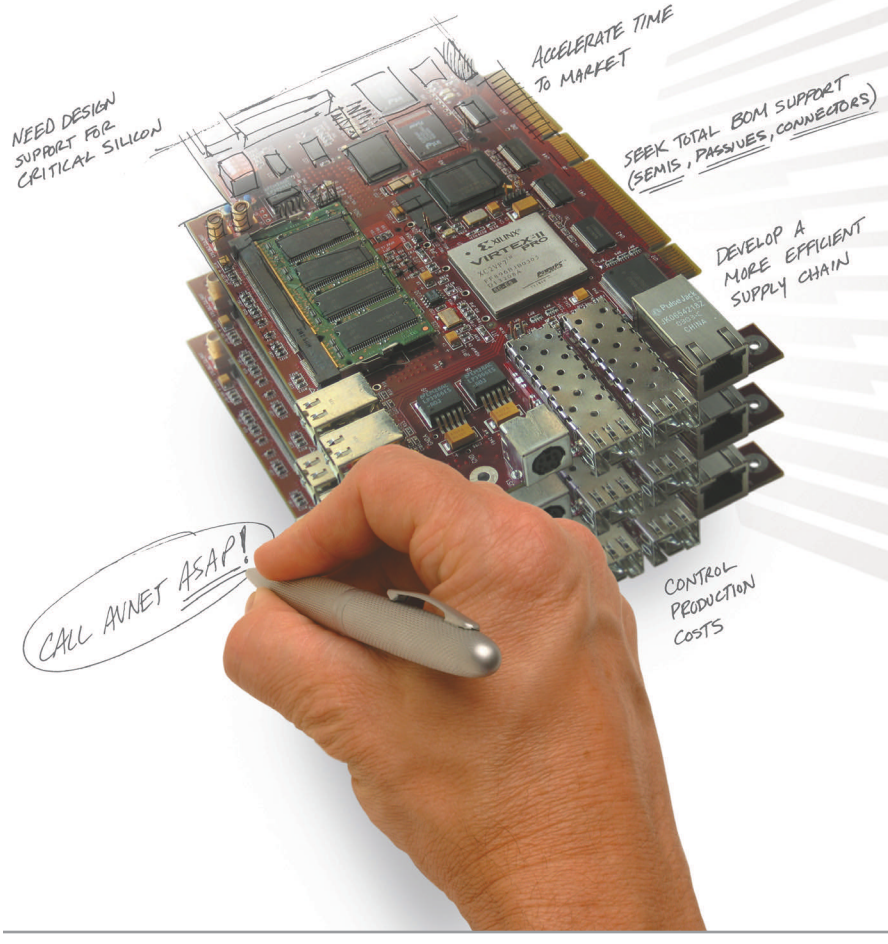

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Ethernet, today's de facto office-networking standard, is increasingly finding its way onto the factory floor. This situation is somewhat surprising, considering that Ethernet's founders never intended it for deployment in such applications. However, its low cost, simplicity, and field-proven open standardization have proved too good to resist.

So, what are the considerations when designing Ethernet into industrial applications? Today's inexpensive, off-the-shelf SOHO (small-office/home-office) Ethernet switches do not provide an acceptable implementation, because they fail to address the unique challenges facing industrial Ethernet: reliability in extreme conditions and deterministic real-time performance.

RELIABILITY IN EXTREME CONDITIONS

The environment for industrial applications may be easy to specify but is by no means easy to design for. Industrial Ethernet covers a multitude of applications that call for conditions of extreme temperatures, high EMC (electromagnetic-compatibility) radiation, and dusty or even wet surroundings.

Industrial-temperature-range Ethernet devices are becoming more common. 100BaseFX fiber support can provide immunity to EMC radiation and longer reach. However, Category 5 cabling still remains the most common physical medium due to its lower cost and robustness compared with fiber. In addition, the standard RJ45 Ethernet connector remains popular, with the alternative M12 connector targeting "watertight" applications.

Traditionally, the weakest link for all Ethernet networks, and not just industrial, has been the physical interface. Issues with installation and maintenance will continue to have a major impact on overall network costs. The role of cable-diagnostics technology, such as TDR (time-domain reflectometry) and VOP (velocity of propagation), goes beyond Ethernet-defined standards to provide relief from these types of problems.

An effective way to expose common cable problems, such as open circuits, short circuits, and impedance mismatches is through TDR. The method involves injecting a pulse of known amplitude and duration down a cable pair and analyzing the reflected pulse. The impedance mismatch at the fault or the load termination causes the reflection. You can use the amplitude of the reflection to calculate the impedance mismatch and determine whether a fault exists down the cable. **Figures 1** and **2** show examples of a reflected waveform for various fault conditions.

You calculate the reflection coefficient, ρ_L, as the ratio of the amplitude of the reflected wave to the amplitude of the incident wave:

$$\rho_L = \frac{V_R\,(\text{REFLECTED WAVE})}{V_I\,(\text{INCIDENT WAVE})} = \frac{Z_L - Z_O}{Z_L + Z_O},$$

where Z_L is the load impedance and Z_O is the cable impedance, which is 100Ω for a Category 5 cable.

By applying this formula, you can easily identify a fault: If $Z_L = 0$, then $\rho_L = -1$ (short). If $Z_L < 100$, then $-1 < \rho_L < 0$ (incorrect termination). If $Z_L = 100$, then $\rho_L = 0$ (correct termi-

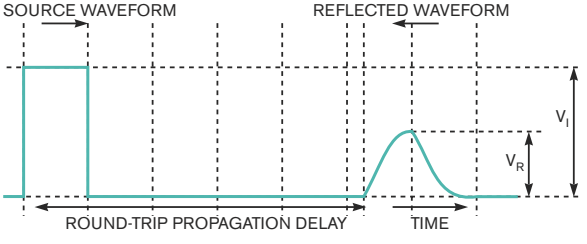

Figure 1 A source waveform reflects when a cable incorrectly terminates.

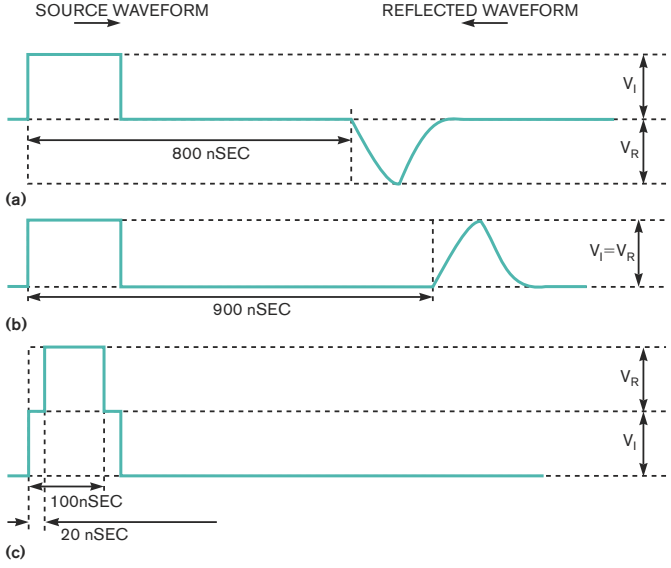

Figure 2 Source waveforms reflect for short (a) and open circuits (b and c) on cables of various lengths.

nation). If $Z_L>100$, then $0<\rho_L<1$ (incorrect termination). If $Z_L>>100$, then $\rho_L=1$ (open). For a perfectly terminated cable, there is no reflection, resulting in $\rho_L=0$. In reality, however, there are always some slight imperfections that occur so you can detect an attenuated reflection.

The significance of the negative-unity reflection coefficient for a short-circuit condition is that the reflection has reverse polarity and equal amplitude relative to the incident pulse (**Figure 2a**). Likewise, for an open-circuit condition, the reflected waveform is of equal amplitude and polarity to the incident waveform (**Figure 2b**), resulting in $\rho_L=1$.

VOP

The VOP specification provides the speed of a signal down a given cable relative to the speed of light in a vacuum (3×10^8m/sec). The VOP specification varies depending on not only the type of cable, but also the manufacturer. The VOP of a Category 5 cable is usually around 0.66. Therefore, a signal travels down this cable at $0.66\times3\times10^8$m/sec$=2\times10^8$m/sec.

Using this specification, you can calculate the length of cable, or distance to fault, by measuring the propagation delay of the reflected waveform. From the previous calculation, a useful rule of thumb for cable length is 5 nsec of propagation delay per meter of cable (remembering to halve the round-trip propagation delay when calculating distance). For example, **Figure 2b** shows the propagation delay of a reflected waveform for a 90m Category 5 cable (open circuit). To calculate the distance to fault:

$$\text{DISTANCE}=\frac{(\text{PROPAGATION DELAY IN nSEC})}{2\times5\ \text{nSEC/m}}.$$

With a propagation delay of approximately 900 nsec, the distance to fault is approximately 90m.

Depending on the implementation, TDR can provide fault diagnostics to a maximum of 200m. Calibration of the VOP for a cabling plant can offer accuracy of ±1m. For cable or fault distances of less than 10m (**Figure 2c**), the reflected wave becomes superimposed onto the original incident waveform. This situation is a result of the propagation round-trip delay

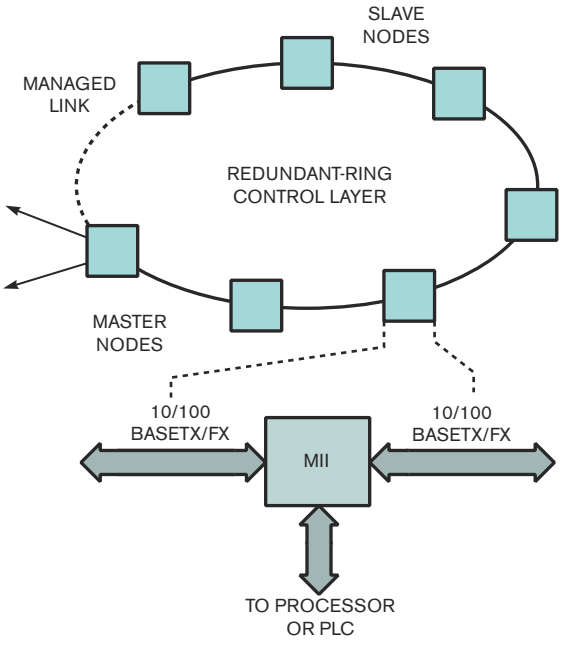

Figure 3 If any link in a redundant-ring topology fails, enabling the managed link can restore the ring.

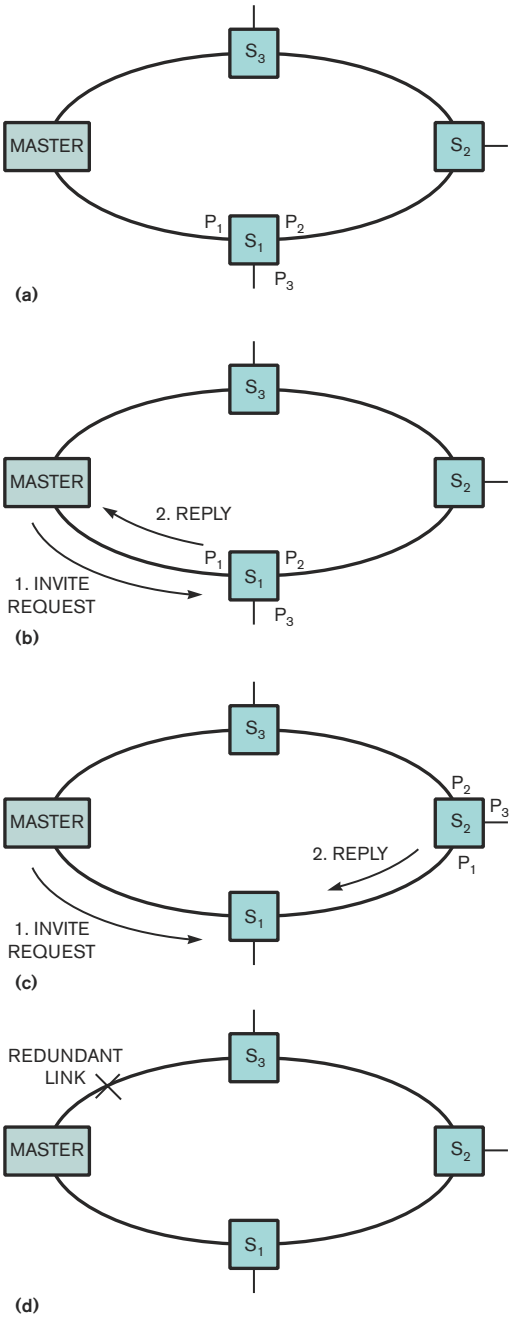

Figure 4 You can use a VLAN to set up a simple redundant-ring network by employing four steps.

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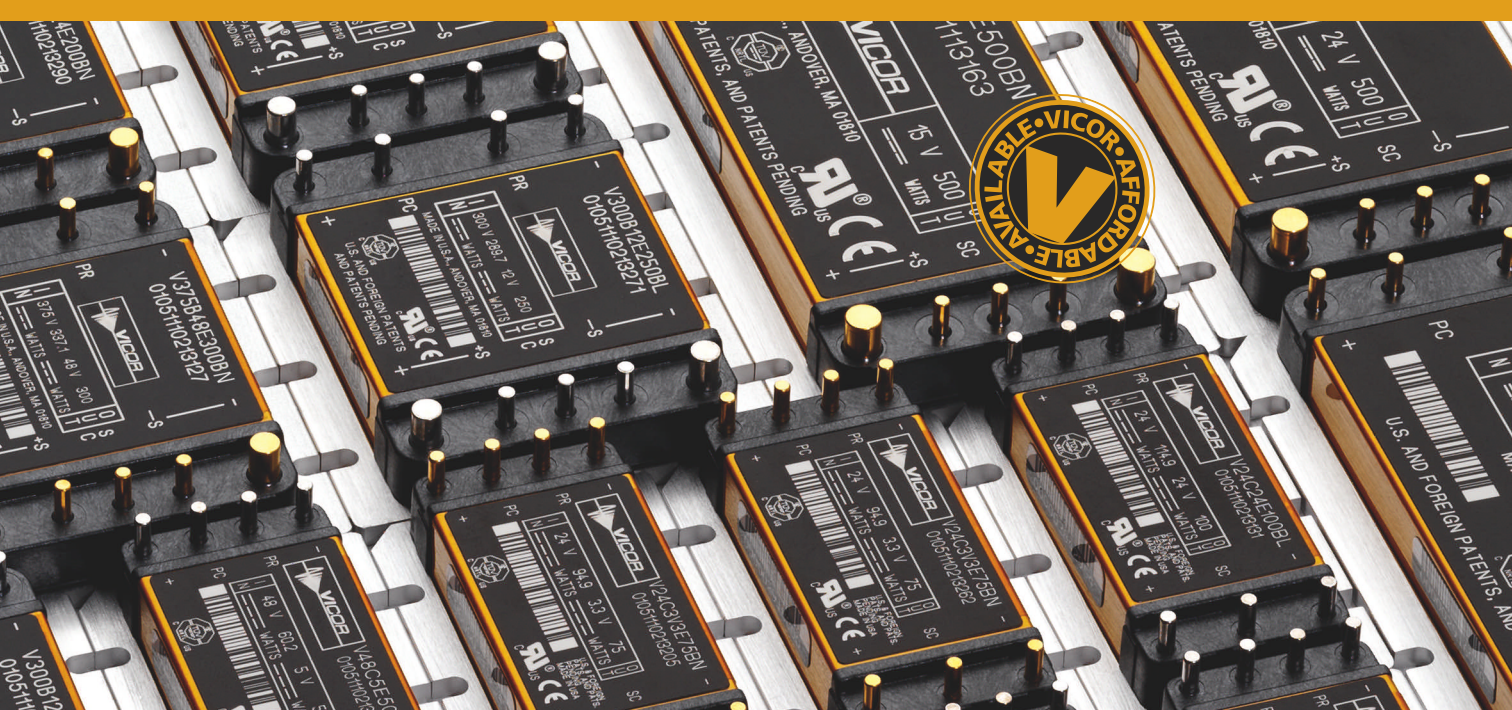

being less than the incident-pulse period: Incident-waveform period (100 nsec)≥cable length×5 nsec/m×2.

REDUNDANT-RING TOPOLOGY

Unlike typical Ethernet "star" networks, in which a multiport switch provides point-to-point links to other nodes, the control layer of an industrial network is usually based on a "redundant ring." This topology eases the logistics of cable installation. Imagine a production line with various sensors distributed along the track. Linking each sensor using a daisy-chain technique simplifies cabling over the method of running a series of longer cables with each routing back to a central switch. To conform to IEEE specifications, the cable can measure no more than 100m. A ring topology limits bandwidth, but this reduction is rarely an issue, because the data rates that automation and control use are usually negligible compared with the higher bandwidths of Ethernet, such as 100-Mbps Fast Ethernet. **Figure 3** shows an example of a redundant-ring control-layer network.

Although you describe such a network as a "ring," it is, in fact, anathema to create any loops within an Ethernet network; hence, you must always break the ring. Failure to break the ring can result in duplication of packets that the system forwards in endless loops, quickly degrading network efficiency. However, this "broken," or "managed," link provides a source of redundancy, because if any of the ring links fail, the system can enable the managed link to again restore the ring.

Although no one has standardized ring management within industrial networks, several higher layer protocols, such as Spanning Tree or Rapid Spanning Tree, are available to identify and break loops in networks. However, you can deploy alternative options using features such as VLANs (virtual LANs). **Figure 4** depicts an example of how to identify and order slave nodes using a VLAN implementation. Here, the master node sends out an "invite request" to each slave node (S_1, S_2, S_3) to capture essential logging information (for example, ID and address). Dynamically configuring each slave node's VLAN settings results in "known" nodes that pass the request through to the next "unknown" slave node in the ring. This unknown slave node forwards the incoming request to Port 3, the processor port, based on the VLAN configuration.

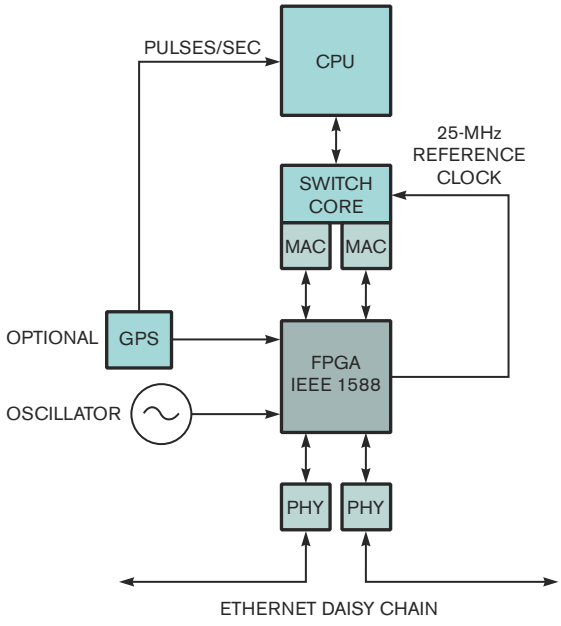

Figure 5 You can implement IEEE 1588 in an Ethernet network using an FPGA.

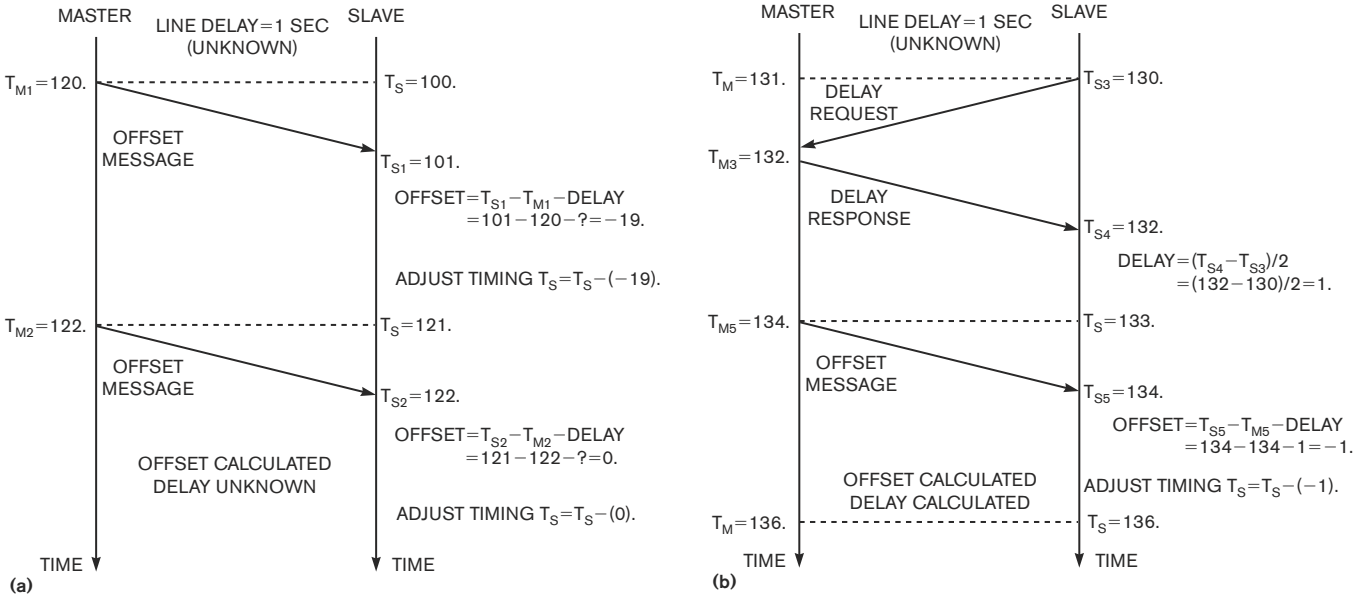

Figure 6 You can calculate the offset (a) and delay (b) phases in the PTP-synchronization process, assuming that the delay between master and slave is symmetrical.

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BRIEF

A 3-A, 1.2-V_{OUT} Linear Regulator with 80% Efficiency and P_{LOST} < 1W

By Jeff Falin • HPA Portable Power Applications

Introduction

Using linear regulators for higher current (>1A), low-output voltage applications has been a challenge for many years due to the regulator's dropout requirements, related inefficiency, cumbersome output capacitor requirements for stability and large inrush currents at startup. The dual input rail TPS74x01 solves these problems.

Linear Regulator Topology Review

The primary drawback of linear regulators for higher current applications is their low efficiency, computed as V_{OUT}/V_{IN}. The power lost (P_{LOST}) in a linear regulator, computed as

$1\text{-}V_{OUT}/V_{IN} * P_{IN} = (V_{IN} - V_{OUT}) * I_{OUT}$,

must be dissipated by its package. The TO-263 or D^2PAK package is the largest surface-mount package in which linear regulators are available. Without additional airflow, its maximum power dissipation capability is approximately 2.75W (assuming it is soldered to a large copper plane for heat sinking). Many higher current "low-dropout" linear regulators with PMOS pass elements have minimum input voltages of 2.5 to 2.7V not only to power the internal LDO drive circuitry but also to drive the PMOS FET hard enough to provide higher output currents.

Therefore, using many PMOS pass element-based linear regulators for output voltages below 1.8V and output currents above 2.5A is cumbersome and costly due to the additional airflow and/or external heat sinking that is required to dissipate the heat generated by the regulator.

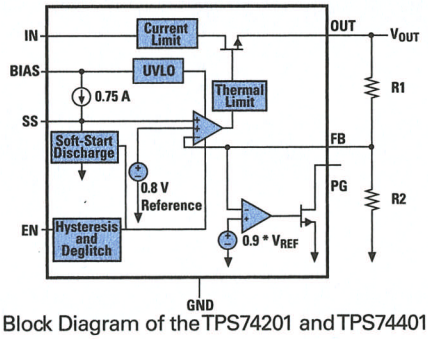

Figure 1. Block Diagram of the TPS74201 and TPS74401 Linear Regulators

Since NMOS FETs have inherently lower RDS_{ON} than similarly current-rated PMOS FETs, an NMOS FET pass element needs less V_{IN}-V_{OUT} drop to provide the same current. However, the source-follower configuration of the NMOS-based regulator requires that the gate of the FET be at least a threshold voltage drop (typically 1V) above the output voltage. The regulator either needs an internal charge pump to provide a higher gate drive voltage, or more simply, a second low-power input rail from an existing 5-V or 3.3-V bias supply. This is the reasoning behind the development of the dual-rail, NMOS pass element-based TPS74x01 family of linear regulators.

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Dropout

As shown in Figure 1, the TPS74x01 regulators have two input voltages, one providing the low current bias voltage to power the internal circuitry that controls the NMOS pass device and a second power input. Since all the internal circuits run off the higher BIAS input, the device is capable of achieving regulation from a low voltage input supply. In fact, the power input, IN, is only limited by the output voltage and dropout of the device.

There are two different specifications for dropout voltage with the TPS74x01. The first specification is referred to as V_{IN} Dropout and is for users who wish to apply an external bias voltage to achieve low dropout. This specification assumes V_{BIAS} is at least 1.62V above V_{OUT}. Such an application might be a low ripple 1.2-V, 3-A power rail for an FPGA transceiver where V_{IN} and V_{BIAS} are provided by 1.5-V and 3.3-V switching supplies, respectively. In this configuration, the 3mm x 3mm QFN package, which is capable of dissipating 1.9W at 55°C, only needs to dissipate

(1.5V - 1.2V) * 3A = 0.9W,

thereby achieving 1.2V/1.5V = 80% efficiency.

The second specification is referred to as V_{BIAS} Dropout and is for users who wish to tie the IN and BIAS pins together. This allows the device to be used in applications where an auxiliary bias voltage is not available or low dropout is not required. Dropout is limited by BIAS in these applications because V_{BIAS} provides the gate drive to the pass FET and therefore must be 1.4V above V_{OUT}. For example, the TPS74201 can provide a 3.3-V, 1.0-A soft-starting (discussed later) supply from a 5-V rail with 3.3V/5V = 66% efficiency and dissipate

(5V - 3.3V) * 1.0A = 1.7W.

Stability and Transient Response

Until recently, linear regulator loop stability presented a challenge to analog IC designers because one of the control loop poles, created by the output capacitor and the impedance at the load, varies in frequency location based on the output current. Regulators with the NMOS pass element in source-follower configuration have always been slightly easier to compensate because their output impedance is lower than a similarly rated PMOS regulator in common-source configuration. This means that the NMOS regulator's moving pole is higher in frequency than the comparably rated PMOS counterpart and so is further away from the internal error amplifier's pole(s). Older methods of ensuring stability were to either roll off the control loop response at low frequency, thereby killing transient response, or counteracting the moving pole with a zero created by an output capacitor with a certain amount of equivalent series resistance (ESR). Using a patented feedback control topology, the TPS74x01 family, configured with V_{BIAS} = 3.3V, V_{IN} = 1.8V and V_{OUT} = 1.5V, achieves fast transient response times (see Figure 2) with no output capacitors but is still stable with larger capacitors having ESR. No output voltage ringing after the load transient shows that the regulator is very stable with no output capacitance.

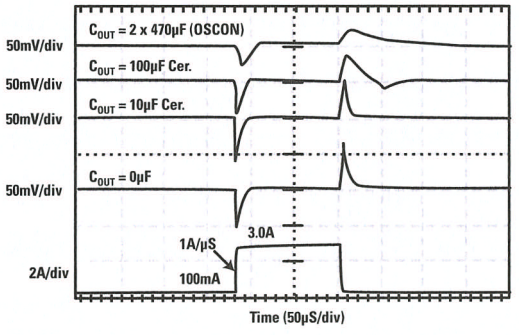

Figure 2. Load Transient Response with Various Output Capacitors

Since the TPS74301 is stable with no output capacitor but has such fast transient response, local bypass capacitance for the device under power may be sufficient to meet the transient requirements of many FPGAs and DSPs, thereby reducing total solution cost by avoiding the need to have multiple bulk capacitors for the power rail.

Soft-Start and Sequencing

Many older linear regulators start up fast because the feedback loop senses the low output voltage and turns the pass-FET on hard. For some applications, fast startup is required; however, such fast turn-on causes large in-rush currents, up to the current limit rating of the device, to charge output capacitors. These large currents may pull down the input power bus and may cause system-level problems. To achieve a linear and monotonic soft-start that reduces peak inrush current during startup and minimizes startup transients seen by the input power bus, the TPS74201 error amplifier tracks the voltage ramp of the external soft-start capacitor until its voltage exceeds the internal reference. The soft-start ramp time is dependent on the soft-start charging current (I_{SS}), soft-start capacitance (C_{SS}), and the internal reference voltage (V_{REF}). It can be calculated using:

$$t_{SS} = (V_{REF} * C_{SS}) / I_{SS}$$

Note that since the soft-start is voltage-controlled, the start-up is not dependent on the output load.

Instead of an SS pin, the TPS74301 version has a TRACK pin. As summarized in Figure 3, with the center tap of a resistor divider from an external supply connected to TRACK, the TPS74301's output voltage will track the external supply until the TRACK voltage reaches 0.8V. This can be used to implement simultaneous or ratiometric sequencing. This feature is useful in minimizing the stress on ESD structures that are present between the CORE and I/O power pins of many processors and/or managing integrated power-on reset circuitry. All members of the TPS74x01 family facilitate implementation of the sequential sequencing by tying the integrated PG signal to the EN pin of a following supply.

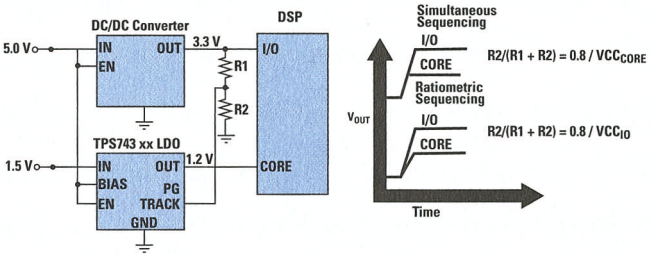

Figure 3. Various Sequencing Methods Using the TRACK Pin

Conclusion

With the dual input rail and low dropout voltage, the TPS74x01 family has made linear regulators more appealing than switching regulators in terms of board size and cost, and comparable in terms of efficiency for powering many lower voltage, higher output current power rails. The family's additional features, including controllable soft starting, tracking and integrated PG, manage startup problems that have plagued linear regulators in the past. Add in the fast transient response, which minimizes the total number of output capacitors, and you have a near-ideal DC/DC converter.

References:

1. TPS74201 Datasheet
2. TPS74301 Datasheet
3. TPS74401 Datasheet
4. Intel App Note AP812 (doc. number 306667 Rev 002)

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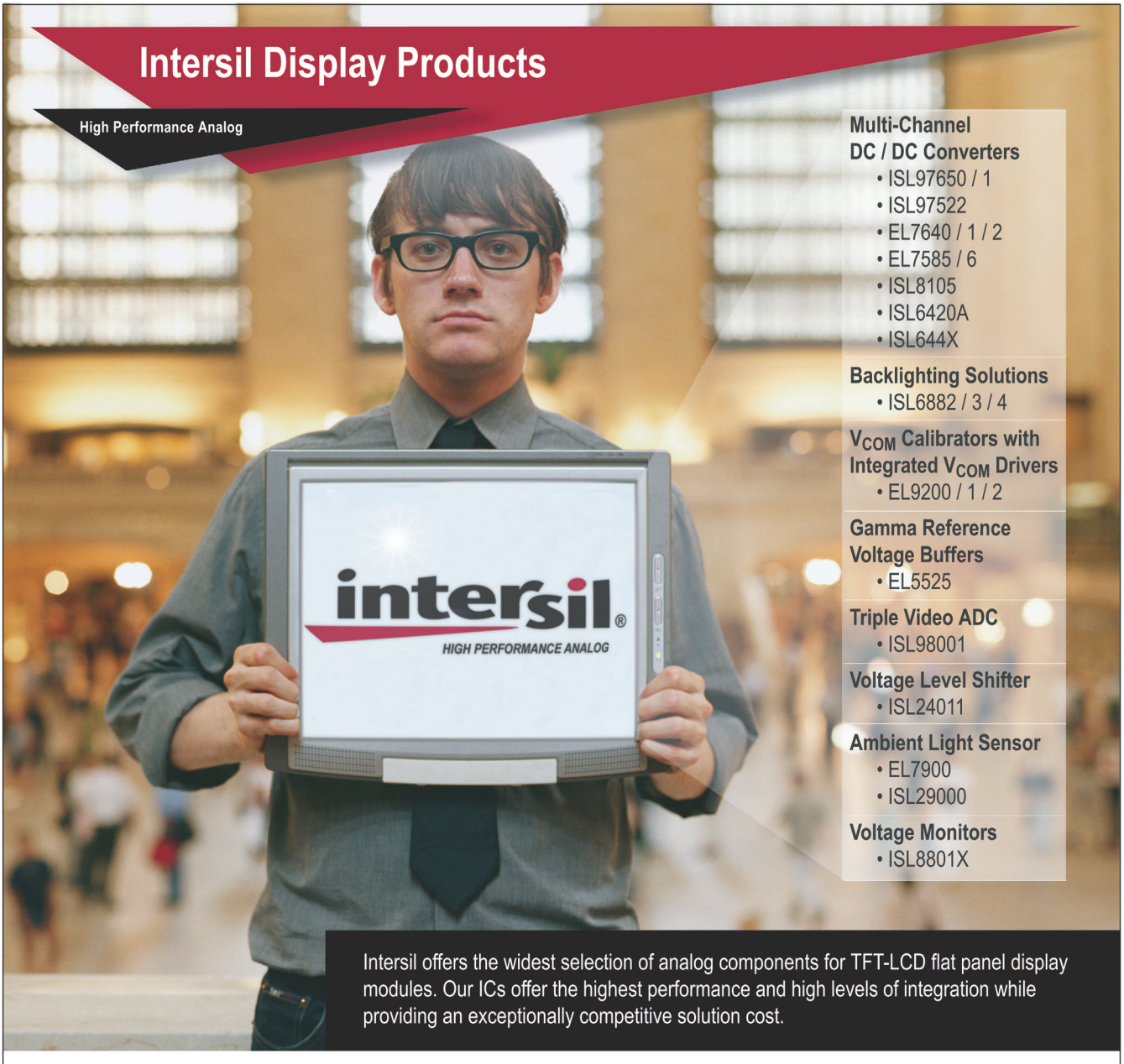

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Redundant-ring topologies are not without their disadvantages. Network latency increases because data must pass through each node in the ring before reaching its destination. Additionally, the store-and-forward architecture of today's Ethernet switches stores packets for processing before forwarding, resulting in nondeterministic latency behavior. **Table 1** shows latency measurements for a five-port switch operating at 100 Mbps over 1m of Category 5 cable. The total latency derives from packet size and the internal forwarding delay. You can calculate this latency as: total latency=(packet size×8)/rate+forwarding delay.

The constant and small forwarding delay that **Table 1** shows is independent of packet size. Hence, fixing the size of the packets in a network provides constant switch latency. To reduce overall switch latency, you should minimize packet size.

To reduce latency jitter in the network, the EPL (Ethernet Powerlink Group) recommends using 100BaseTX/FX Ethernet repeater hubs. Repeater hubs employ a cut-through architecture that significantly diminishes latency by forwarding incoming packets to all ports except the ingress port before all packets have arrived, providing lower latency than store-and-forward switches, independent of packet size.

You can realize another approach to the deterministic delivery of packets through the use of higher level protocols, such as IEEE 1588. IEEE 1588 uses UDP (User Datagram Protocol) packets over IP (Internet Protocol) on the Ethernet network to provide synchronization in a network that is accurate to within 1 µsec. Such performance fulfills the stringent real-time requirements for motion-control applications. ProfiNet, Ethernet/IP, and the industrial-Ethernet groups have all adopted this standard for network synchronization. **Figure 5** shows a typical hardware implementation of the IEEE 1588 functions using an FPGA.

To achieve synchronization with the rest of the network, each node must determine which clocking source to use. All nodes perform the "best-master-clock" algorithm to select a timing source. If a node is to be a master to many nodes in the ring, then the design must use a high-precision source, such as a GPS (global-positioning-system) device. If the node is not a master, it extracts timing information from the network using the IEEE 1588 protocol. If a timing source is unavailable from the network, the system requires an onboard oscillator to provide a local timing source. The master is responsible for notifying all slaves in the network of its position. If a slave does not receive any such notification, then it designates itself as the master.

TABLE 1 LATENCY MEASUREMENTS FOR A FIVE-PORT SWITCH

Packet size (bytes)	Total latency (µsec)	Forwarding delay (µsec)
64	7.6	2.5
128	12.9	2.7
256	23.1	2.7
512	43.7	2.8
1024	84.7	2.6
1280	105.1	2.7
1518	124.2	2.8

Note: based on measurements using a KSZ8995MAI Micrel industrial five-port switch operating at 100 Mbps over 1m of Category 5 cable.

To synchronize the master and slaves, IEEE 1588 uses the PTP (Precise Time Protocol) based on IP multicasting and requires the FPGA and switch core to identify PTP packets. The FPGA adds a time stamp to ingress and egress PTP packets. In the ingress direction, the switch then forwards incoming PTP packets directly to the CPU port. Time-stamping occurs after the SOF (start of frame) at the first bit of the DA (destination address). Using PTP enables Ethernet networks to synchronize to within less than 1 µsec.

Alternatively, you can implement IEEE 1588 in software to avoid the need for an FPGA. In this scenario, the processor performs time-stamping. However, it can be difficult to compensate for the nondeterministic latency of the switch, typically resulting in a 10- to 100-µsec reduction in synchronization accuracy. Consequently, software-based time-stamping is unsuitable for precision applications, such as motion control.

The IEEE 1588-synchronization process first calculates and corrects the offset time between the master and slave. To perform this function, the master continuously transmits a unique message to the slave at defined intervals, usually every 2 sec. The second phase of the synchronization process is the delay measurement. The slave sends a delay request to the master that the system returns; it then calculates the round-trip delay using the time stamps. This scenario assumes that the delay between the master and the slave is always symmetrical. **Figures 6a** and **6b** provide an example of the offset and delay phases of the PTP-synchronization process.

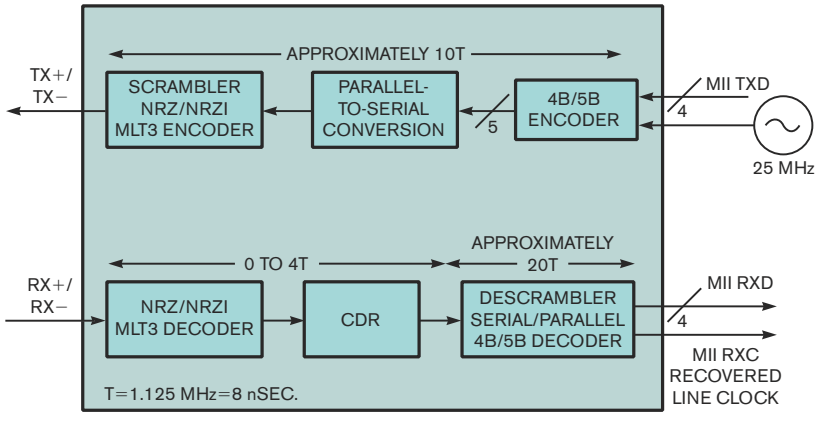

Figure 7 By analyzing the basic building blocks of a PHY with an MII, you can estimate the latency jitter introduced into the network.

MII OR RMII?

The standard Ethernet MAC/PHY (media-access-control/physical-layer) interface is the MII (media-independent interface), whether you are implementing a system using an FPGA, a network processor, an Ethernet switch, or a PHY. This interface, which IEEE 802.3u defines, comprises 16 pins for data and control signals (a 4-bit data bus operating at 25 MHz). To reduce the pin count for multiport FPGA-, ASIC-, or

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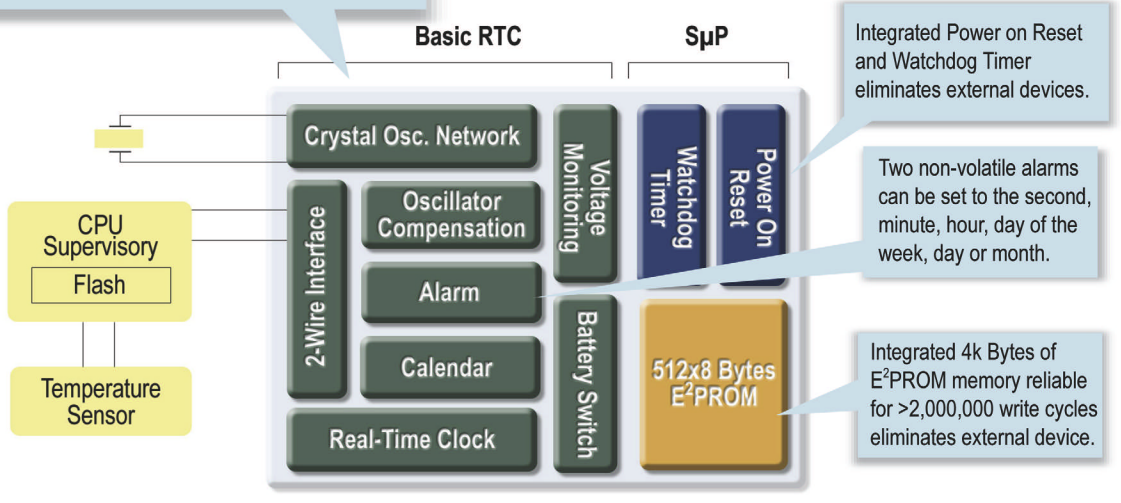

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800nA General Purpose Real-Time Clock Selector Table

	Int. E²PROM (Bytes)	Alarm	CPU Sup.Fx's POR	CPU Sup.Fx's Wdg Timer	IRQ	FOUT	VTRIP for Rest/Bat Switch	Package
ISL12026	512 X 8	2	N	N		IRQ/FOUT	5 Sel. (2.63V to 4.64V)	8-Ld SO/TSSOP
ISL12027	512 X 8	2	Y	Y		RESET	5 Sel. (2.63V to 4.64V)	8-Ld SO/TSSOP
ISL12028	512 X 8	2	Y	Y		IRQ/FOUT	5 Sel. (2.63V to 4.64V)	14-Ld SO/TSSOP
ISL12029	512 X 8	2	Y	Y		IRQ/FOUT	5 Sel. (2.63V to 4.64V)	14-Ld SO/TSSOP

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processor-based designs, a vendor-led consortium introduced the RMII (reduced-MII) specification. RMII provides independent 2-bit-wide transmitting and receiving paths synchronized to a common 50-MHz reference clock, reducing the total interface pin count to eight.

However, MII is still the preferred interface for real-time applications. People rarely appreciate that RMII does not replace MII but adds a reconciliation layer on either side of MII. Moving from the recovered incoming line clock to the RMII reference clock requires a FIFO to tolerate differences in frequency. The result is an increase in latency jitter, the bane of all real-time networks.

Analyzing the basic building blocks of a PHY with MII or RMII reveals the typical latency jitter that the network sees (**Figure 7**). This implementation-independent analysis ignores any variations due to process and temperature.

In the transmitting direction, data synchronizes to a local 25-MHz oscillator and typically adds a fixed delay of approximately 80 nsec. Unlike the receiving direction, in which there is a variable delay due to the clock recovery, alignment adds to a fixed delay of 160 nsec. The variable delay is due to the alignment of the generated 25-MHz MII receiving clock with respect to the recovered 125-MHz line clock, which results in an offset of five possible phases: 0, 8, 16, 24, or 32 nsec. PLL-recovered clock jitter may also add 10 nsec to the total receiving-path latency.

Variable delays are more critical than fixed delays in a real-time network, because they are unknown; therefore, you cannot compensate for them. Using the MII, an Ethernet PHY typically exhibits a round-trip delay of approximately 240 to 282 nsec, thus adding as much as 42 nsec to overall network-latency jitter.

Additional latency occurs when interfacing to

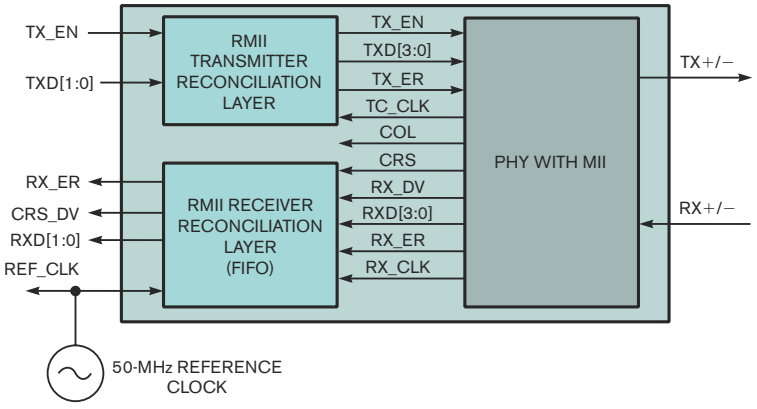

Figure 8 Estimating the latency jitter for RMII requires taking into account the reconciliation layer between RMII and MII.

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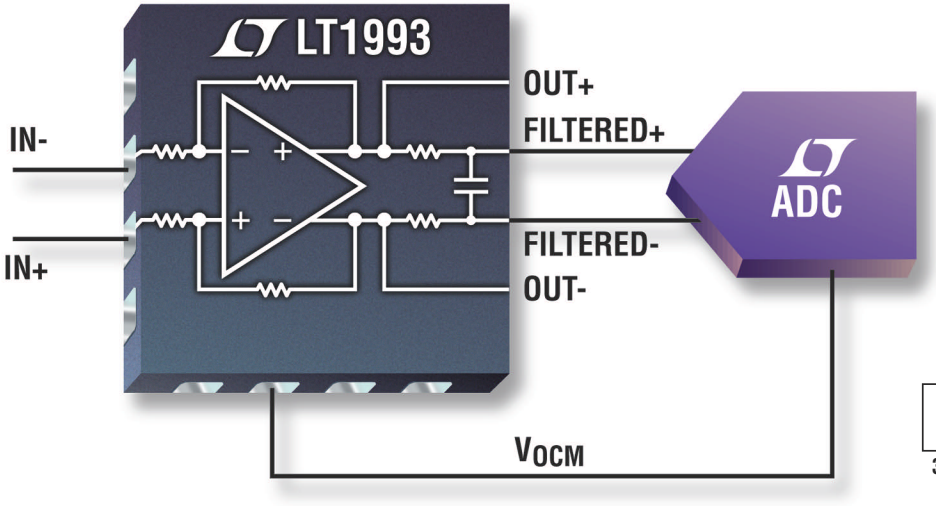

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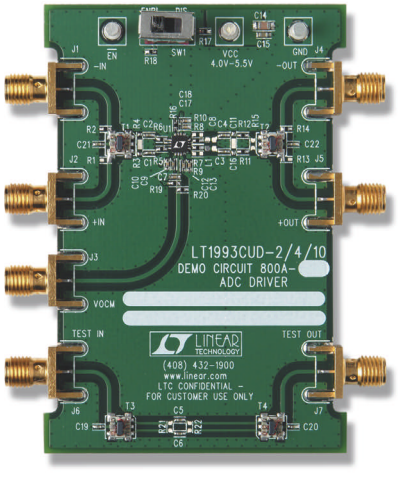

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the Ethernet PHY through RMII, due to the reconciliation layer (**Figure 8**). In the transmitting direction, like MII, the PHY uses the reference clock as the network clock. Hence, the added delay is, perhaps, only a single 50-MHz clock cycle. This situation does not occur in the receiving direction when the reconciliation layer needs to account for the differences between the local reference clock and the recovered clock. Typically, an implementation uses a FIFO. The RMII specification advises using a 20-bit-deep FIFO with transfer of the recovered data onto RXD[1:0] when the FIFO is half-full. Such a design consequently adds as much as 200 nsec of latency jitter in the receiving path, in addition to MII latency. However, you can regard this recommendation as a minimum.

Many vendors design their silicon to operate in a far more robust timing environment—100 ppm (0.01%)—than what the IEEE specifies. For example, Cisco Systems designs equipment to cope with frequency errors as high as 0.1%, which is not uncommon in today's networks. This demand increases the required FIFO size to 27 bits and the maximum RMII latency jitter to 27×10 nsec=270 nsec: FIFO size (bits)=2×(maximum frame size)×(network error+local error)=2×(1518×8)×(0.1%+0.01%)=26.7 bits.

Another PHY/MAC interface standard, the SMII (serial-MII), has recently started to become popular among processors, FPGAs, and Ethernet transceivers. SMII is similar to RMII but has fewer pins—receiving, transmitting, synchronizing, and reference clock—operating at 125 MHz. Again, the need to retime the incoming recovered line clock onto the synchronous reference clock requires an elastic buffer. As with RMII, the result is increased latency jitter.

Industry experts widely agree that Ethernet will eventually replace the traditional field bus for device-level industrial communications. Certainly, this replacement will not happen overnight, but, in the short term, Ethernet will operate in parallel before eventually superseding the field bus, providing customers with the most efficient, lowest cost road map.

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The challenge of designing Ethernet into such harsh environments and providing the necessary deterministic, real-time performance is demanding. However, by making the right architectural decisions and through careful implementation, you can successfully meet these goals. EDN

AUTHOR'S BIOGRAPHY

Michael Jones is a field-applications engineer with more than 10 years of high-tech design experience in the semiconductor industry. He is currently based in Newbury, UK, where he is responsible for Micrel Semiconductor Ltd's European applications for high-speed networking and Ethernet products. Jones holds a degree in electronic-systems engineering from Aston University (Birmingham, England), and his writings have been published in a variety of technical and industry publications worldwide.

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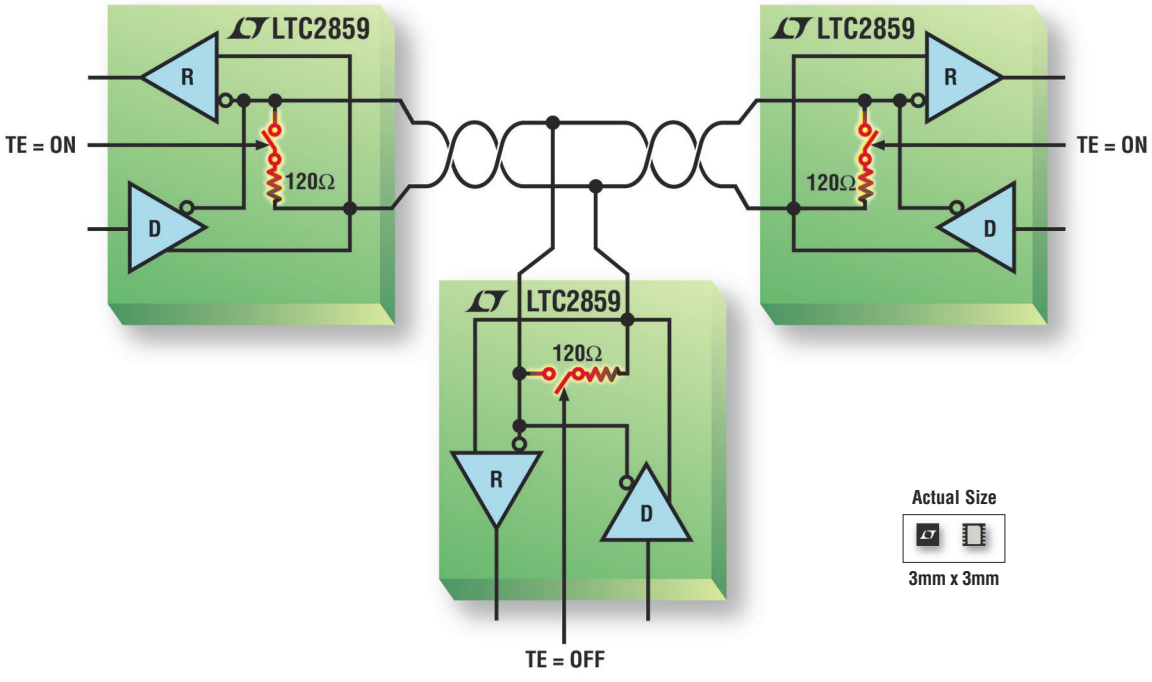

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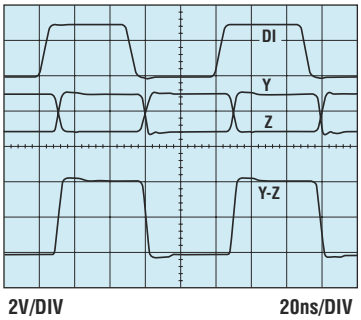

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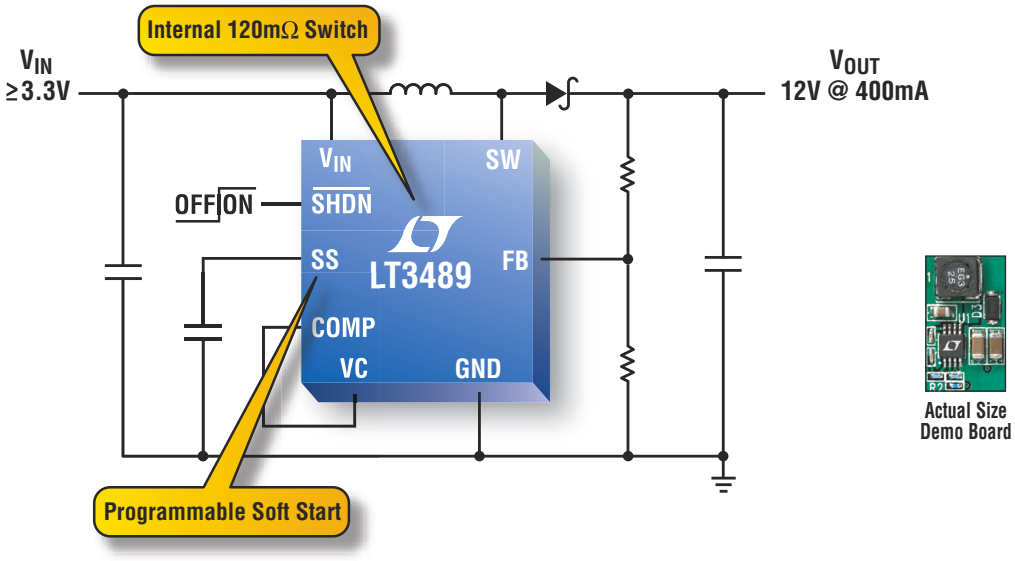

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LT3479	2.5V to 24V	40.0V	3A	3.5MHz	4mm x 3mm DFN-14 TSSOP-16E
LT1370HV	2.7V to 30V	40.0V	6A	500kHz	TO-220, TO-263

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Ultralow-cost, two-digit counter features few components

Noureddine Benabadji,
University of Sciences and Technology, Oran, Algeria

The ultralow-cost, two-digit-counter circuit in **Figure 1** represents an attempt to reduce the number of components using a mostly software approach and a low-cost microcontroller, the PIC16F84A. The circuit lacks the current-limiting resistors that normally connect to a seven-segment LED display's pins because a software routine lights only one of the display's segments at a time, first in the 10s display and then in the units display. Doing so keeps the circuit's maximum current consumption at a nearly constant level, even if you add a third LED display to implement a three-digit counter. The circuit also lacks digit-selection switching transistors that classic multiplexed circuits' switching transistors typically use, and the circuit includes one common-cathode and one common-anode display. The reason for this approach is that each of the microprocessor's I/O Port A and Port B lines can assume one of three states: high, low, and floating—that is, high impedance. Programming a line as an input places it in a high-impedance state, which turns the display off.

In addition, the program drives only one segment at a time and executes the following sequence: To drive the 10s display, program the line RB0 output and drive it high to light the corresponding segment of the common-cathode display and then program RB0 as an input. Repeat this procedure for lines RB1 through RB6. To drive the units display, repeat the process while applying a low output from RB0 to drive the common-anode display. **Figure 2** shows the circuit's timing diagram. The prototype display uses Kingbright's (www.kingbright.com) SC52-11EWA (DS_1) and SA52-11EWA (DS_2) high-efficiency, seven-segment displays that emit 2000 to 5600 µcd at a forward current of 10 mA. At a forward current of approximately 5 mA, the displays remain readable.

Early motion pictures displayed at an 18-Hz rate, which produces marginal flicker. The software executes at a rate of 180 Hz, or 10 times the minimum flicker rate. Each of the display's seven segments must illuminate for an interval of 1/(180×7) sec, or approximately 0.8 msec. To simplify the timing routine (section Delay3 of **Listing 1**, available at www.edn.com/060817di1), the software uses a refresh interval of 1 msec.

Although this approach provides adequate segment-drive current, the display's internal LEDs carry a 3V maximum reverse-voltage rating. Driving any I/O line high applies forward bias to one segment of the common-cathode digit but applies reverse bias to the

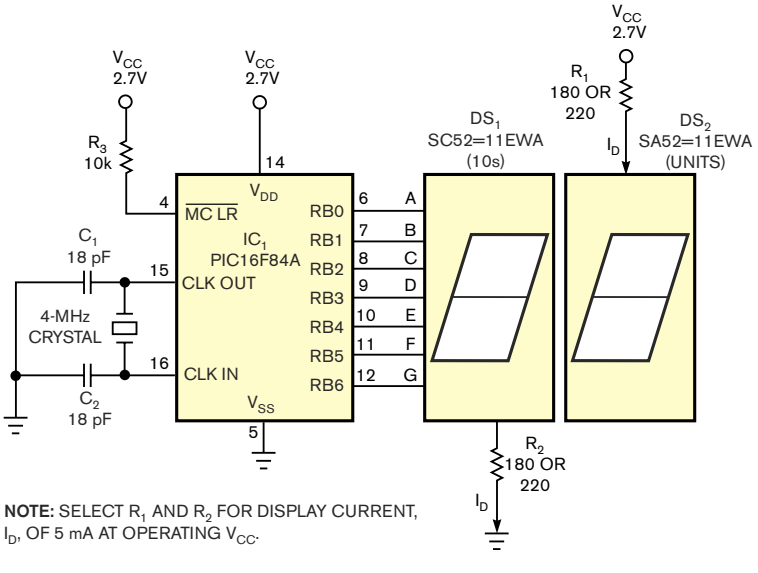

Figure 1 This low-cost, two-digit counter uses few components.

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corresponding segment of the common-anode display. The 16F84A requires a minimum of 2V for operation, and thus the circuit must operate in a 2 to 3V power-supply range. The assembler source code in **Listing 1** counts from 0 to 99 sec and serves as an unoptimized proof-of-concept software test bed for the display.EDN

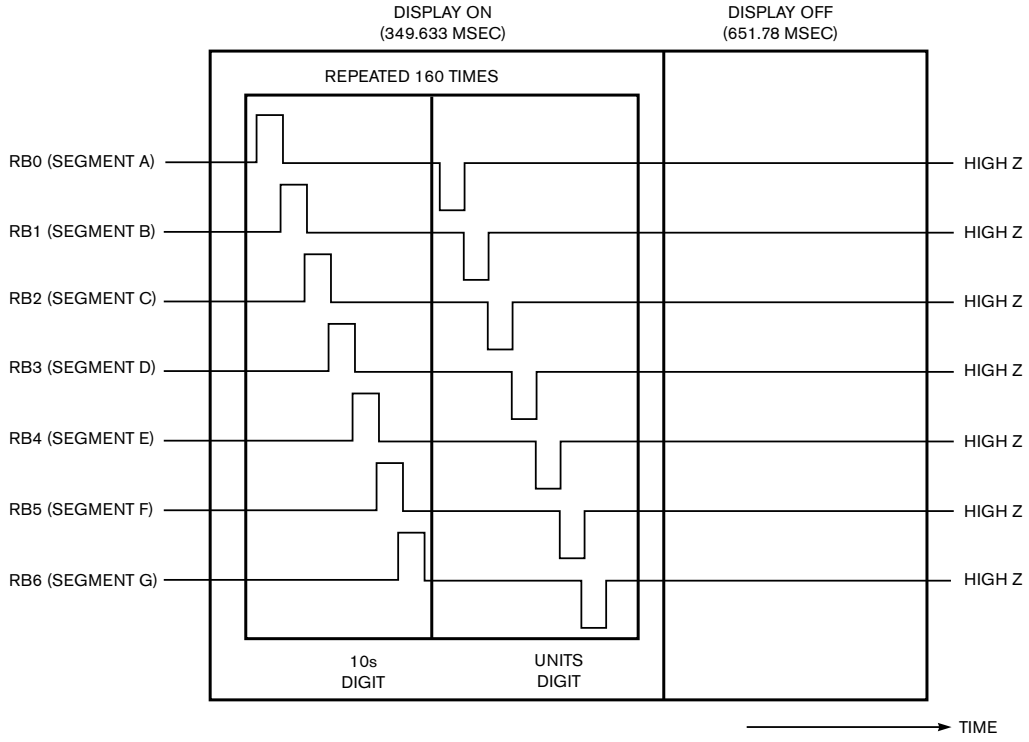

Figure 2 The timing diagram illustrates segment- and digit-drive intervals.

Two-wire, four-by-four-key keyboard interface saves power

Stefano Salvatori, University of Rome, Rome, Italy,
and Gabriele Di Nucci, EngSistemi, Rome, Italy

You can use a microcontroller that includes an ADC to design a two-wire-plus-ground keyboard interface. For example, you can use a resistive voltage divider to identify a pressed key (**Reference 1**). A microcontroller's integrated ADC typically presents an input resistance on the order of hundreds of kilohms, and, for adequate accuracy, its keypad divider should comprise relatively low-value resistors of 10s of kilohms. However, in battery-powered systems, a resistive divider can consume a few hundred microamperes, forcing a designer to choose an alternative classic digital-matrix array of switches and multiple I/O lines. Moreover, portable-equipment designs typically place constraints on the number of components.

To satisfy both requirements, the circuit in **Figure 1** uses a matrix keypad and a resistor network divided into two row and column sections. For the four-by-four-key keypad, seven resistors are sufficient to encode any pressed key, and the circuit consumes power only while a key remains closed. Conversely, with no keys pressed, the standby current approaches zero. Using only two values of resistors, let $R_A=R_B=R_C=R_1$ and $R_D=R_E=R_F=R_G=R_2$. Assigning values from zero to three for the keys' x and y addresses, you can calculate the voltage across resistor R_G for any key closure by solving the following **equation**:

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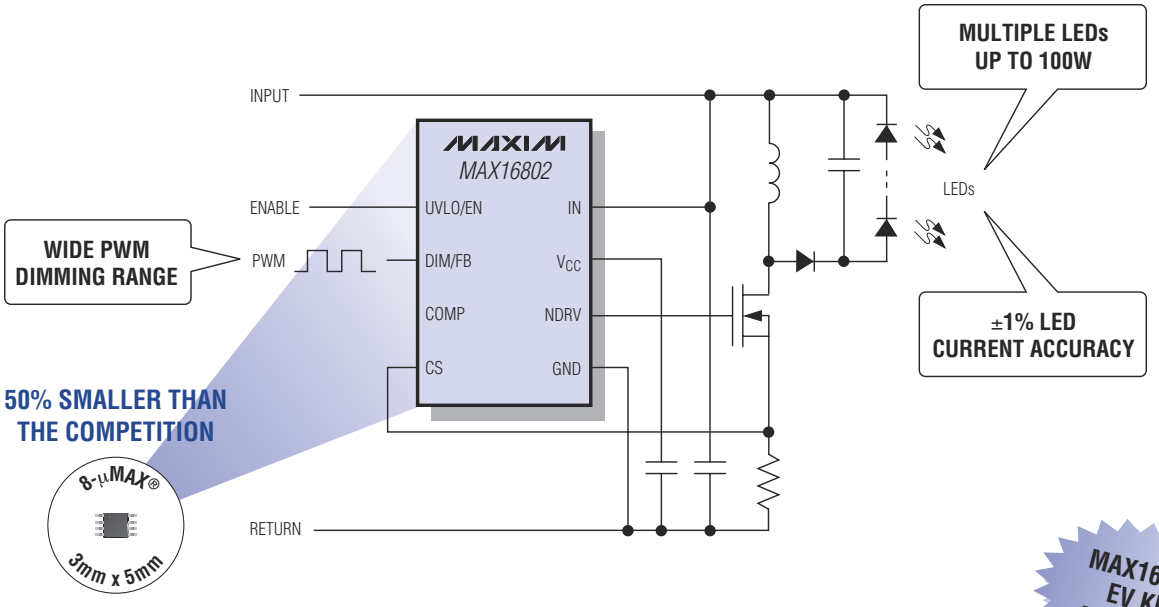

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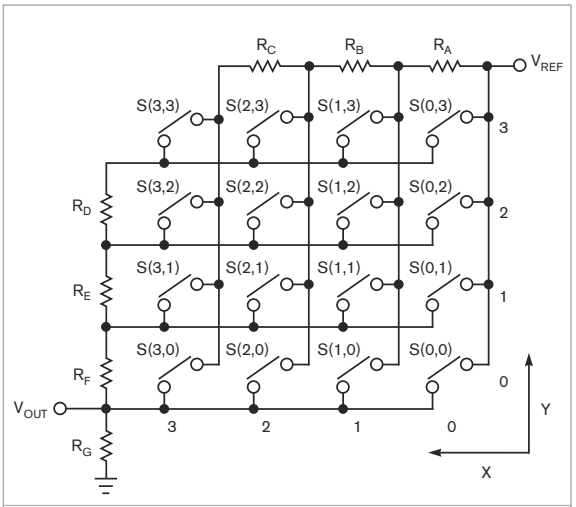

Figure 1 A two-wire resistive voltage-divider interface encodes a four-row-by-four-column keypad.

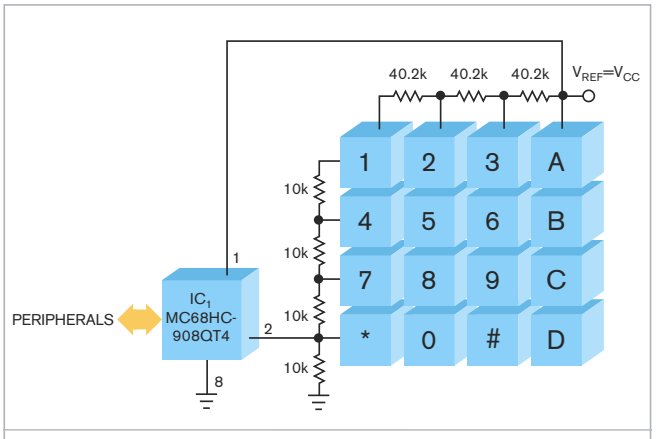

Figure 2 Using the microcontroller's analog reference-voltage output and ratiometric analog-to-digital conversion ensures correct encoding of the keypad.

TABLE 1 SINGLE-KEY OUTPUT CODES

Keys pressed/resistance (Ω)				
	X			
Y	3	2	1	0
	1/	2/	3/	A/
3	15 to 16	21	32	63 to 64
	4/	5/	6/	B/
2	17	23	36	85
	7/	8/	9/	C/
1	18	25	42	127
	*/	8/	#/	D/
0	19	28	51	255

Note: The figures preceding the slashes represent the keypad's key labels.

TABLE 2 TWO-KEY OUTPUT CODES

Keys pressed	Resistance (Ω)
C+#	141 to 142
C+0	134 to 135
C+*	132
B+#	109
B+0	98
B+9	91
B+8	88
A+8	76
A+7	70 to 71
A+6	68

$$V(x,y)=V_{REF}\times\frac{R_2}{x\times R_1+y\times R_2+R_2}.$$

Driving the resistor array from V_{REF}, the ADC's reference voltage, allows you to perform a ratiometric conversion that eliminates errors in key encoding due to fluctuations in V_{REF}. The following **equation** describes the voltage-division ratio, r(x,y), for any keystroke.

$$r(x,y)=\frac{V(x,y)}{V_{REF}}=\frac{1}{(1+x\times p+y)}.$$

The ratio $p=R_1/R_2$ represents the ratio between row- and column-group resistors' values. For p=4, you calculate 16 values of r(x,y), in the [1/16, 1] range, as a function of the pressed key's position. In general, the minimum difference between r partitioning ratios occurs for the nearest keys as the (3,2) and (3,3) x,y indexes indicate. For an N-bit ADC and a ratio of p=4, the ADC should have a resolution that satisfies the following **equation**: $2^{-N}<r(3,2)-r(3,3)=15^{-1}-16^{-1}=240^{-1}$. Note that the reciprocal of 240 (0.0041...) exceeds the reciprocal of 2^8, and the circuit thus requires an ADC capable of at least 8-bit resolution ($N\geq 8$ bits).

Unfortunately, standard-value components with nominal tolerance, T, cannot provide an ideal solution to this **equation**. Instead, you calculate a partitioning-ratio difference, $d=r(3,2)-r(3,3)$, for the worst-case condition. The lowest value of d occurs for a minimum value of R_G and R_D and the maximum value of R_A, R_B, R_C, R_E, and R_F. You can account for all the resistors' values and define a generic ratio, p, for the nominal values of R_1 and R_2:

$$d_{MIN}(p,T)=(1-T)^2/\{[3\times(p+1)+(3p+1)\times T]\times[(3p+4)+3\times p\times T]\}>2^{-N}.$$

The same value of T applies to all resistors. If n=8 and p=4, the previous **equation** yields a solution of T<0.018, which indicates that resistors of ±1% tolerance correctly encode 16 keys. Moreover, if you now impose the chosen fixed tolerance, T, you can solve the **equation** to obtain the required limit on the p ratio between the values of R_1 and R_2. If T=0.01, the solution to the **equation** becomes p<4.074.

The circuit in **Figure 2** uses Freescale's (www.freescale.com) Nitron MC68HC-908QT4 microprocessor, which serves as a test bed for a keypad based on the above-calculated values, and uses pow-

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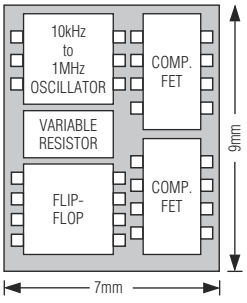

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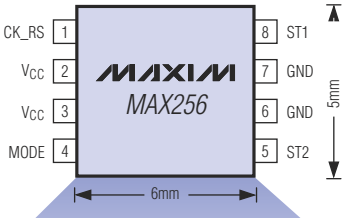

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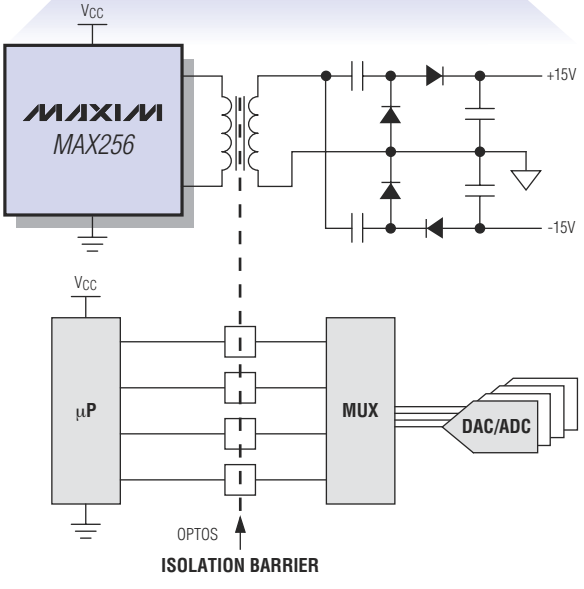

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er-supply voltage V_{CC} as the resistor matrix's reference voltage, V_{REF}. To satisfy the requirement for p(4.074 >p>4), use R_1=10 kΩ±1% tolerance and R_2=40.2 kΩ±1% tolerance, both standard values that the E48 series offers. **Table 1** lists output codes corresponding to 16 individually pressed keys, and **Table 2** lists data obtained when simultaneously pressing two keys and illustrates that two-key combinations can evoke special functions.

If your application requires a microcontroller that lacks an internal interrupt that the ADC generates, you can connect an external comparator to the output voltage in **Figure 1**. Set the comparator's threshold lower than the lowest voltage developed at the output voltage—approximately V_{REF} divided by 16 in the example—and the comparator's output serves as a keypad-interrupt source for the microcontroller.

Note that a microcontroller with a 10-bit ADC, such as a Freescale MC68HC908QB or a Texas Instruments (www.ti.com) MSP430F11 can service a five-row by six-column keypad matrix encoded by 10 resistors. Repeating the analysis shows that a row-to-column p ratio of 5 to 5.51 and a required resistor tolerance of less than 4.3% correctly encode the keys. You can use values of 10 kΩ for R_1 and 51.1 kΩ or 53.6 kΩ for R_2 of the ±1%-tolerance E48 series.

REFERENCE

1 Amorim, Vitor, and J Simões, "ADC circuit optimizes key encoding," *EDN*, Feb 4, 1999, pg 101, www.edn.com/article/CA56657.

Gain-of-three amplifier requires no external resistors

Marián Štofka, Slovak University of Technology, Bratislava, Slovakia

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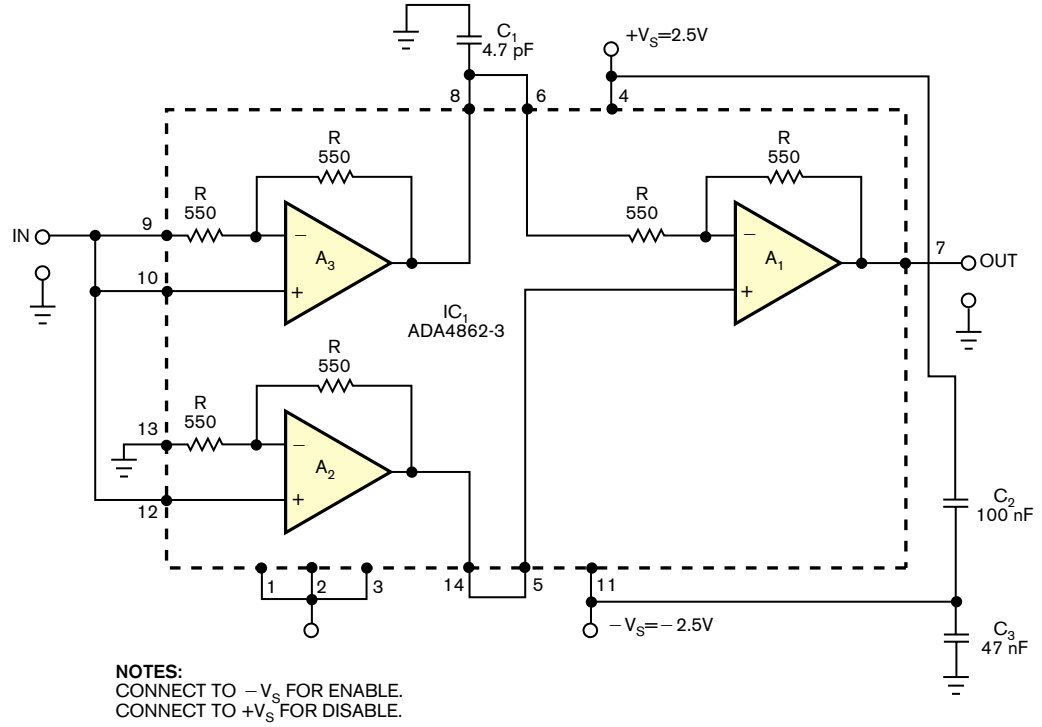

Figure 1 A one-IC amplifier with a voltage gain of three provides flat response to more than 60 MHz.

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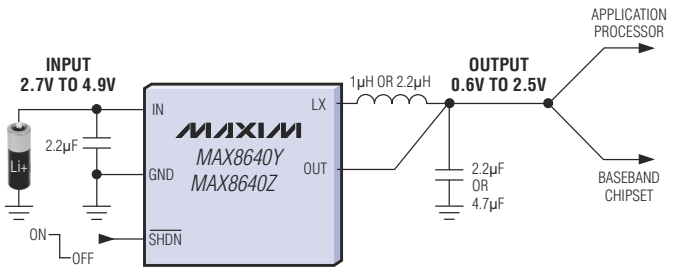

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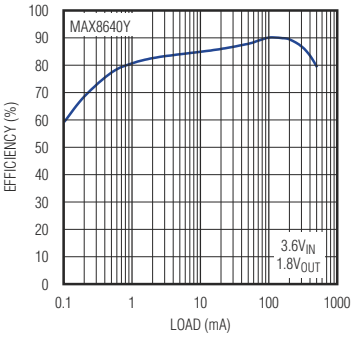

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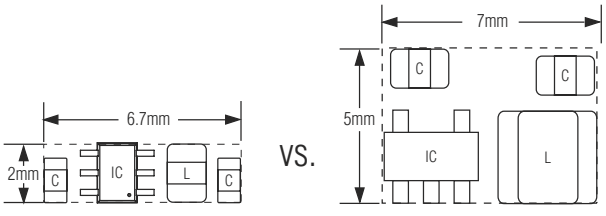

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three gain configurations—two, one, or negative one (**Reference 1**). When you configure it for a gain of two, a cascade of two or three amplifiers yields gains of four or eight, respectively. If your application requires a gain of three, you can use the circuit in **Figure 1**. Amplifier A_3 serves as an impedance converter with a net voltage gain of one and a low-impedance driver for A_1's gain-setting network. Amplifier A_2 provides a gain of two at its noninverting input.

In addition, A_3 introduces the proper time delay (phase shift) in A_1's inverting-input path and thus roughly equalizes the time delay in A_1's noninverting signal path. This configuration improves the circuit's dynamic performance over that you can achieve when A_1's inverting input connects directly to the input signal. A 4.7-pF chip capacitor that connects from voltage follower A_3's output to ground reduces the voltage follower's output impedance at frequencies of 100 MHz and above to ensure A_1's stability.

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If you configure it as a differential amplifier, A_1 amplifies the input signal by a factor of two at its noninverting input and by a factor of negative one at its inverting input. The final voltage at A_1's output comprises the algebraic sum of both components: $V_{OUT}=4\times V_{IN}-V_{IN}=3\times V_{IN}$. In a conventional voltage amplifier, reducing negative feedback increases the overall gain. In contrast, cascading amplifiers with negative-voltage-feedback networks only slightly reduces the circuit's bandwidth. The net gain decrease at a frequency of 65 MHz amounts to 0.1 dB, or approximately 1.15% of a single gain-of-two amplifier's dc gain. For the gain-of-three amplifier in **Figure 1**, the gain decrease at 65 MHz amounts to approximately 2.3% of the circuit's dc gain.

For the best high-frequency performance, connect the ADA4862's internal amplifiers as **Figure 1** shows to minimize the lengths of the device's external interconnections. You can cascade additional ADA4862-3 ICs to produce any gain expressed as $3^M\times 2^N$, where M and N represent integers, including zero—that is, gains of six, nine, 12, and so on. EDN

REFERENCE

1 ADA4862-3 data sheet, Analog Devices Inc, www.analog.com/UploadedFiles/Data_Sheets/360747397ADA4862_3_a.pdf.

LINEAR TECHNOLOGY

DESIGN NOTES

Universal Li-Ion Battery Charger Operates from USB and 6V to 36V Input in Just 2cm^2 – Design Note 395

Liu Yang

Introduction

There are a number of advantages to offering USB and high input voltage power and battery-charging capability in handheld devices such as GPS navigators, PDAs, digital still cameras, photoviewers and MP3 players. For instance, charging and operation from USB offers the obvious convenience of not requiring a travel adapter. High voltage sources, such as Firewire and 12V to 24V adapters are even better, since they provide faster charging than USB and allow charging in more places, such as in the car. Nevertheless, there is an important design consideration with high voltage power sources: the voltage difference between the high voltage source and the battery in the handheld is very large. Since a linear charger cannot handle the power dissipation, a switching charger is required.

The LTC®4089 and LTC4089-5 (see Figure 1) conveniently integrate a high voltage and wide input range (6V to 36V with 40V absolute maximum) monolithic 1.2A buck switching regulator and a USB power manager/charger into a compact thermally enhanced 3mm × 6mm DFN package. The LTC4089's buck regulator output voltage tracks the battery voltage to within 300mV. This Bat-Track™ feature minimizes overall power dissipation. The LTC4089-5 has a fixed 5V at OUT when power is applied at HVIN. When power is supplied from the USB port, the power manager maximizes the available power to the system load; up to the full USB available power of 2.5W. It automatically adjusts the Li-Ion battery charge current with respect to the system load current to maintain the total input current compliance within the USB limits. The total solution size is less than 2cm^2 with all components on one side of the PCB.

Adaptive High Voltage Buck Minimizes Total Power Loss

The LTC4089's buck converter output voltage V_{OUT} tracks the battery voltage V_{BAT}. It is always 0.3V higher than V_{BAT}, so that the battery can be charged quickly while

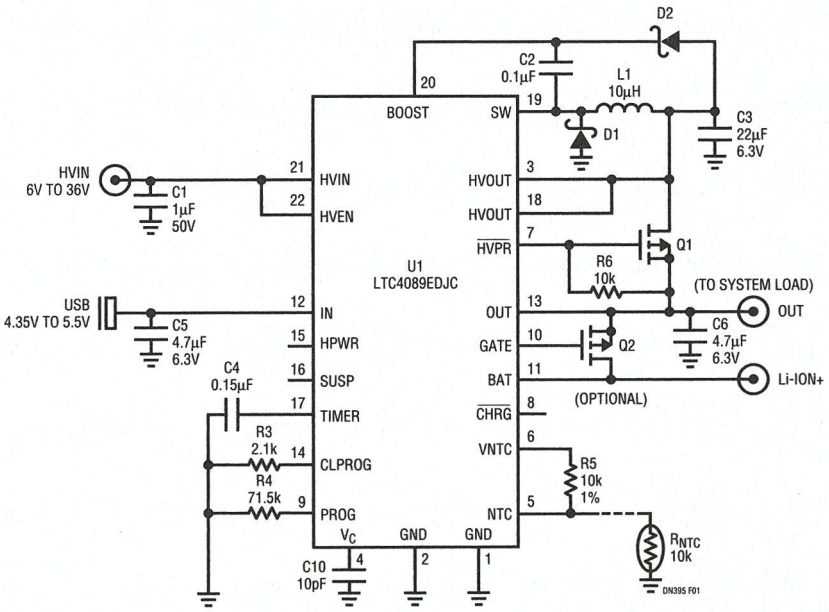

Figure 1. The LTC4089 Schematic Illustrates Multiple Input Voltage Capability

minimizing overall power dissipation. Figure 2 shows the overall efficiency at various input voltages, where the total power dissipation is less than 1.1W. Furthermore, if the battery is excessively discharged and V_{BAT} falls too low, the minimum V_{OUT} is 3.6V to ensure continuous system operation.

USB Power Manager Maximizes Power Available to the System

In a traditional dual input device, the input charges the battery and the system's power is directly taken from the battery. This creates a number of problems. One of these is that the system's available power is reduced by the low-battery voltage when there is USB power present. For example, when V_{BAT} = 3.3V, the available power to the system is only 1.65W while the USB itself supplies 2.5W. The balance is dissipated as heat. The LTC4089 successfully solves this problem by providing an intermediate voltage V_{OUT} to power the system load.

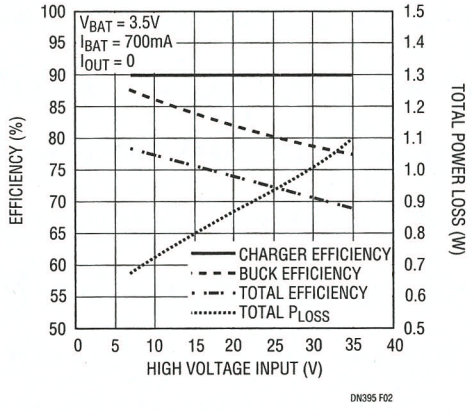

Figure 2. The LTC4089 High Voltage Charger Efficiency and Total Power Loss

This V_{OUT} is independent of the battery voltage and equal to the USB voltage, thus the full USB power is available to the system load. Table 1 shows the advantages of the LTC4089 power manager over the traditional dual input configuration.

Small Footprint

With all the necessary components on the same side of the PCB, the total solution size is less than 2cm^2 (11.3mm × 17.5mm) as shown in Figure 3.

Summary

The LTC4089 integrates a high voltage wide input monolithic switching regulator, USB power manager and Li-Ion battery charger into a 3mm × 6mm DFN package and improves the functionality of USB-based and multiple power input portable devices.

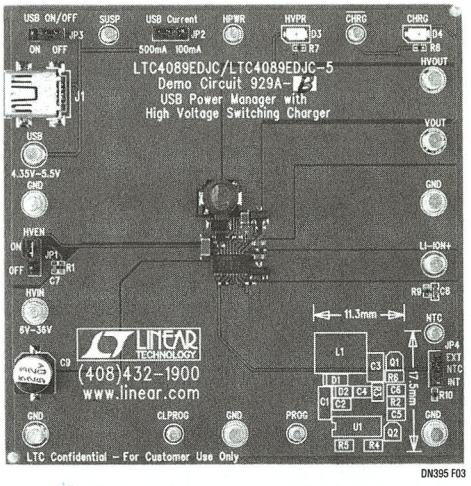

Figure 3. The LTC4089 Demo Circuit with Layout in Bottom Right Corner

Table 1. Comparison of Traditional Dual Input Charger and Linear Technology's LTC4089 Power Manager/Charger for USB Charging

SCENARIO	TRADITIONAL DUAL INPUT CHARGER	LTC4089 POWER MANAGER/CHARGER
Battery voltage is below trickle charging voltage	Available current to system is only trickle charge current (50mA to 100mA), which may not be sufficient to start the system	Full adapter/USB power is available to system, although battery is in trickle charge
Battery is not present	Most chargers consider this as a fault. The system cannot start	Full adapter/USB power is available to system
V_{BAT} = 3.3V at USB input	Available power to system is only 1.65W. The system power cannot be greater than this	Full 2.5W USB power is available to the system
System consuming close to the input power limit	Cannot distinguish the available charging current. Charger timer runs out before the battery is fully charged	Charger time proportionally increases with less available charge current. The battery is always fully charged

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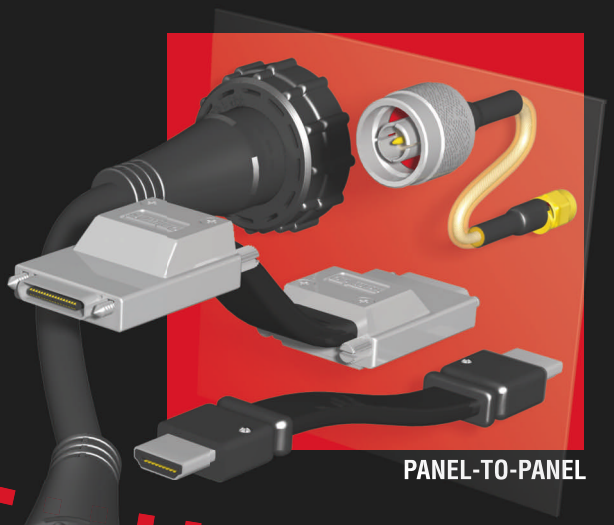

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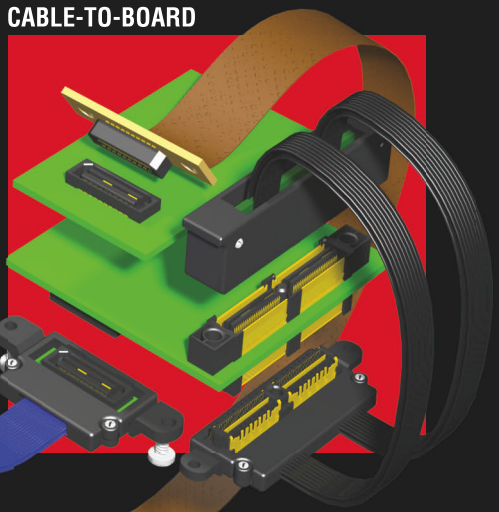
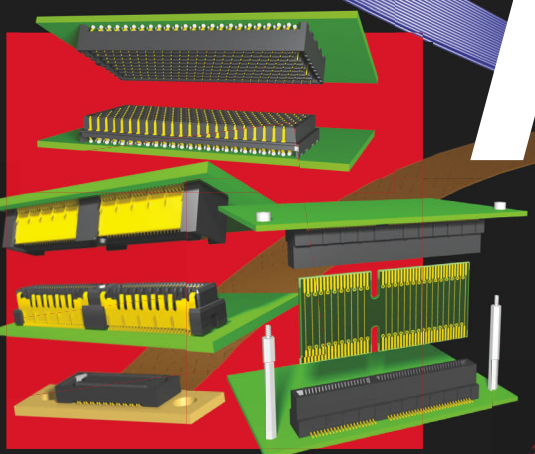
PANEL-TO-BOARD

CABLE-TO-BOARD





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SWITCHES AND RELAYS

Self-protected electronic fuse targets inrush-current-limiting applications

Using a high-side N-channel FET driven by an internal charge pump, the NIS5112 integrated, self-protected, resettable electronic fuse suits use in 12V systems in hot-swap applications, including enterprise-class hard drives. An internal sensing FET enables active current limiting using inexpensive chip resistors in place of low-impedance current shunts, and an adjustable voltage-slew rate allows designers to select the level at which the current limits and the rate at which the output voltage rises. Available in an SO-8 package, the NIS5112 costs $1.15 (2500).

On Semiconductor, www.onsemi.com

Switch catalog and CD-ROM feature selector guide

The full-line switch-products catalog and companion CD-ROM list panel-mount rocker switches, navigation switches, and the C&K Elum illuminated pushbutton switches. The disk also includes ROHS (reduction-of-hazardous-substances) part numbers and application information. A selector guide on the CD allows engineers to quickly find the most suitable switch series. Additional features include technical data, soldering guidelines, contact material, drawings, and packaging information. A downloadable version of the catalog and CD is available at the vendor's Web site.

ITT Industries, www.ittcannon.com

USB 2.0 switch features high ESD protection

The 480-Mbps, high-speed FSUSB31 USB 2.0 switch features 8-kV ESD (electrostatic-discharge) protection. Targeting port isolation in ultraportable systems, the FSUSB31 features a 6.5-pF on-capacitance, a 2.5-pF off-capacitance, and the ability to handle a 720-MHz bandwidth. In addition, the device draws 1 µA and protects against excessive capacitance, noise, and other factors negatively affecting performance. Available in a 1.6×1.6-mm package, the FSUSB31 switch costs 90 cents (1000).

Fairchild Semiconductor, www.fairchildsemi.com

SPDT analog switches feature a low on-resistance

Combining a 0.4Ω on-resistance and a 1.6 to 4.3V operating range with DFN-10 and MSOP-10 packages, these dual-SPDT (single-pole/double-throw) monolithic CMOS-analog switches suit signal-routing applications in portable and battery-powered end products. The DG2731, DG2732, and DG2733 switches target cell phones, PDAs, portable media players, speaker headsets, hard drives, and modems. The DG2731 and DG2732 feature separate control pins with reverse-control logic; the DG2731 has two NO (normally open) and two NC (normally closed) switches, the DG2732 has three NO switches and one NC switch, and the DG2733 has two NO switches, two NC switches, and an enable pin to enable the device when the logic is high. The SPDT analog switches cost $1.40 (1000).

Vishay, www.vishay.com

Ultralow-distortion units switch between data and audio signals

The ISL54400, ISL54401, and ISL-4402 family of audio/data switches includes both high-bandwidth, low-

productroundup

SWITCHES AND RELAYS

capacitance and low-distortion, low-capacitance models. The switches suit USB-data downloading and 20-mW/channel MP3-encoded stereo-audio playback. Features include a distortion-negative-signal capability of 20 mW/channel into 32Ω, detection of bus voltage on the USB cable, and generation of the termination voltage for USB D+ and D− pullup resistors. The devices are available in 2.1×1.6×0.5-mm uTQFN and 3×3×0.75-mm TDFN packages. In a DFN-10 lead package, the ISL54400, ISL54401, and ISL54402 cost $1.07, $1.04, and 79 cents, respectively.

Intersil Corp, www.intersil.com

MICROPROCESSORS

Upgrade supports Windows Mobile 5.0

Version 8.02 of the WinDriver USB/PCI driver-development-tool kit supports Windows Mobile 5.0 and Linux kernels 2.6.14 to 2.6.16. Aiming at cross-operating-system and multiple-architecture-host-driver development, the upgrade also supports WinDriver USB devices for USB-firmware code generation. The WinDriver USB-device firmware-development kit supports the Silicon Laboratories C8051F340 development board. A free, three-day evaluation version of WinDriver USB/PCI is available at the vendor's Web site.

Jungo Software Technologies, www.jungo.com

Hydraulic-control system simulates controller and plant models

Simulating hydraulic-control systems within the Simulink environment, the SimHydraulics system allows developers to simultaneously model and simulate controllers and plant models. Joining the SimPowerSystems, SimMechanics, and SimDriveline lines of modeling tools, the software provides a library of common hydraulic fluids and hydraulic building blocks to calculate pressure and flow through standard and nonstandard components. Features include modeling and simulation of the conversion of hydraulic power into driving torques and forces for mechanical motion, the effects of opening and closing valves, and simple mechanical components. Available for Microsoft Windows, Unix/Linux, and Macintosh platforms, the SimHydraulics package cost $4000.

The Mathworks, www.mathworks.com

Hardware platforms enhance software performance

The QuickTransit hardware-virtualization platforms allow Solaris/SPARC applications to run without source-code or binary changes on Linux/Intel Xeon- and Itanium 2-based servers. The platforms allow the fully functioning applications to run with transparent interactive and graphics performance and enhanced computational performance.

Transitive Corp, www.transitive.com

Multimedia starter kit features SDK CD

With support from the vendor's VisualDSP++ 4.5 integrated software-development and -debugging environment, the Blackfin multimedia starter kit includes the ADSP-BF561 EZ-kit Lite evaluation hardware and software, the EZ-Extender daughtercards, and the Blackfin SDK (software-development-kit) CD. The SDK CD features multimedia-software code for rendering and capturing video and audio streams with various off-the-shelf multimedia devices. The

MICROPROCESSORS

kit features multimedia algorithms, including JPEG, MJPEG, Ogg Vorbis, Speex, and SRGP (Simple Raster Graphics Package), as well as Blackfin- and PC-communication drivers and utilities. The VisualDSP++ 4.5 features a compiler-commentary track offering logical improvement suggestions to streamline code and to connect or disconnect enhancements from the target board for added stability. Additional features include a scriptable flash-memory programmer and added exposure and access to hardware breakpoints. Users who own the Blackfin EZ-kit Lite, USB-LAN EZ-Extender, and Audio-Video EZ-Extender daughterboards can download the SDK for free. Upgrading to Version 4.5 is free to registered VisualDSP++ users and licensed EZ-kit Lite users.

Analog Devices, www.analog.com

EDA TOOLS

Integrated-design environment uses a hierarchical database

Targeting the high-volume-IC market, the Unity integrated-design environment combines the UniPlan floorplanning tool, the UniPlace placement tool, the UniRoute routing tool, and the UniEdit editing tool with signal integrity and timing into a consistent database. Based on a hierarchical database, the physical-design platform features legacy CDBA (Cadence-database-access) and Open Access compliance, eliminating mixed-signal "spaghetti" flows. UniPlan features automatic block placement of soft and hard macros, suiting mixed-signal design. Nonintegrated-design flows must separate the design into analog and digital parts; the vendor claims that Unity suits these needs with a flow capacity of several million cells, compared with the vendor's previous version's 200,000-cell capacity. Unity also provides the smallest area and highest yield for mixed-signal and custom digital design. The Unity tool set costs $70,000.

Pulsic Ltd, www.pulsic.com

IC tool's upgrade adds I/O sequencing

Version 3.0 of RioMagic's package-aware IC-design tool supports rules-driven I/O-sequencing and -prototyping, wire-bond, and flip-chip features. Version 3.0 permits users to specify ESD (electrostatic-discharge) clamping, filler cells, gasket cells, or other special cells upfront in the design process. RioMagic costs $199,000 per year for a three-year, time-based license.

Rio Design Automation Inc, www.rio-da.com

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STATS Named one of the worst tech products of all time / Sony subsequently copied it

Palm PCs: micro PC or macro failure?

Way back in 2000, a few friends working at Apple decided to leave and create a palm-sized computer that would run Windows XP. They called the company Oqo. The product used a low-power Transmeta processor, and the prototype employed a 12-layer circuit card that Ken Bahl, the owner of Proto Express in Sunnyvale, CA, said was his proudest achievement that year. However, the venture capitalists didn't quite see the utility of the product. So Oqo never got the big infusion of cash it needed. *PC World* was no kinder when it named the product 19th in its list of the "25 Worst Tech Products of All Time." (AOL was No. 1.)

Now, Sony has introduced the VAIO UX series. It slides open just like the Oqo, and its price ($1800) is comparable. The UX has a 1.2-GHz Intel processor, a 30-Gbyte hard drive, and 512 Mbytes of memory. It incorporates a 1024×600-pixel, 4.5-in. screen; Bluetooth; 802.11a/b/g; and wireless WAN using Cingular's network. Its two cameras include a Web cam and a conventional outward-facing camera.

VAIO and Oqo are both compelling because you can use them as Internet phones. Both have Bluetooth and 802.11 capability. And with Skype, a leading voice-over-Internet Protocol service provider, you could sit down with one of these micro PCs at any modern café and call anywhere. So, is the micro PC a viable platform or just geek jewelry?—by Paul Rako

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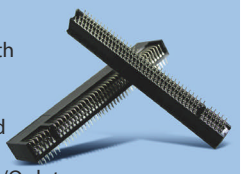

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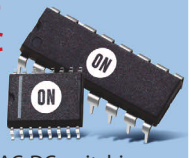
ON Semiconductor MC33 Series AC-DC Switching Off-line Controllers



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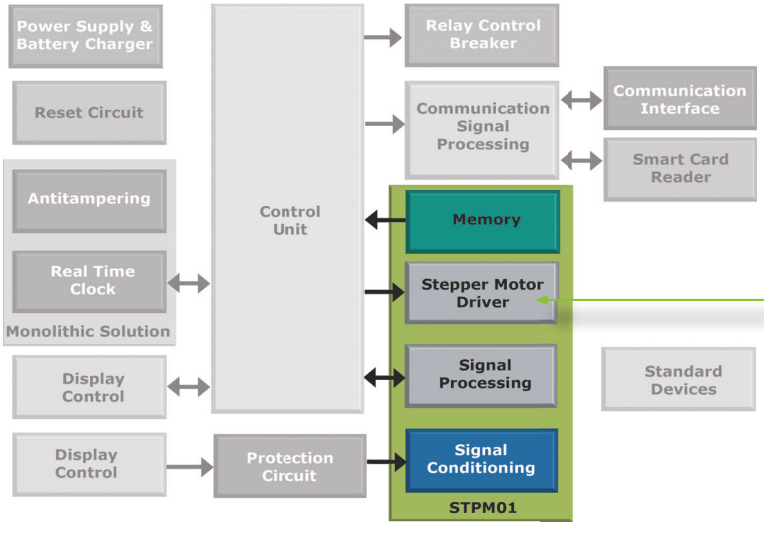
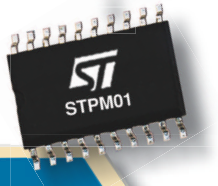
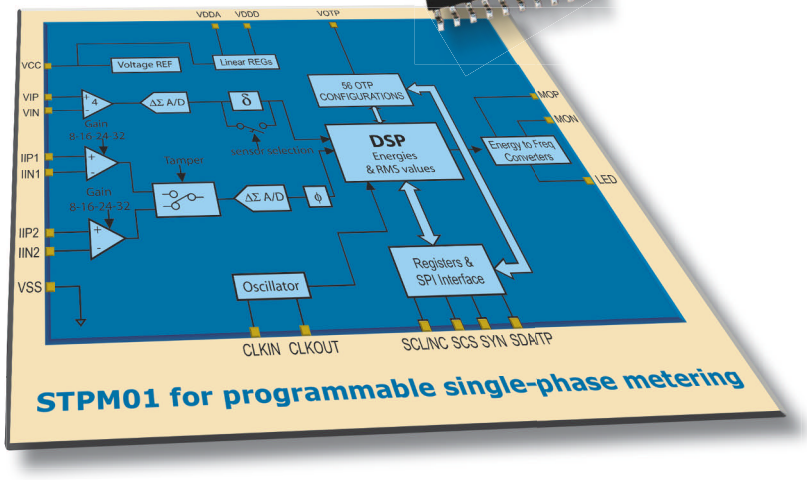


ST complements its vast range of standard devices with world-beating innovative segment specific products like the STPM01. Designed for effective energy measurement in power line systems utilizing Rogowski coil, current transformer and/or shunt sensor, it can measure active, reactive or apparent energy; RMS and instantaneous voltage and current consumption or line frequency via an SPI communication bus.





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- Support 50÷60Hz, IEC 62052-11 and IEC 62053-2x specifications
- Less than 0.1% error
- Precision voltage reference: 1.23V and 30 ppm/°C max

For further information, datasheets and application notes visit www.st.com/stpm01

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